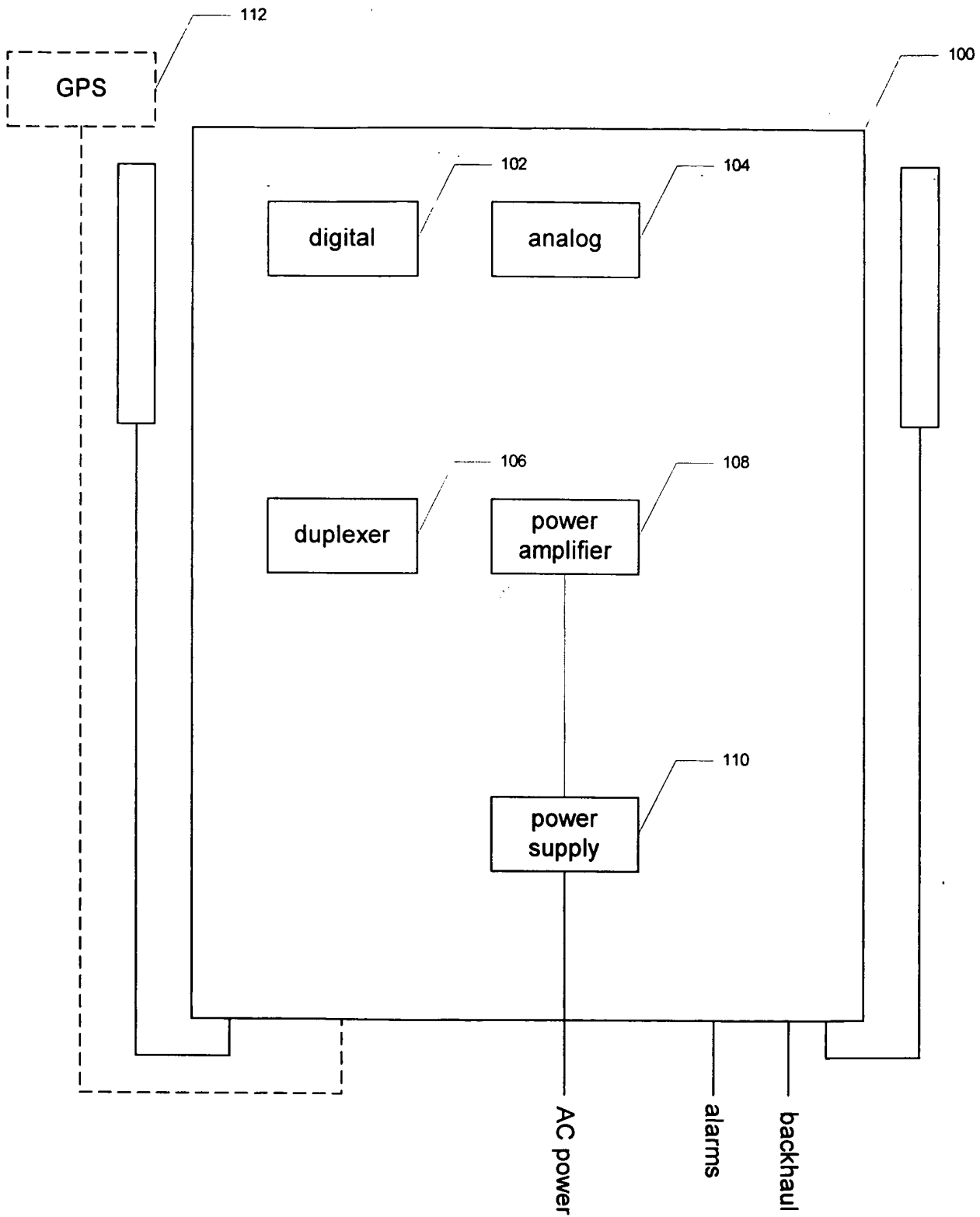
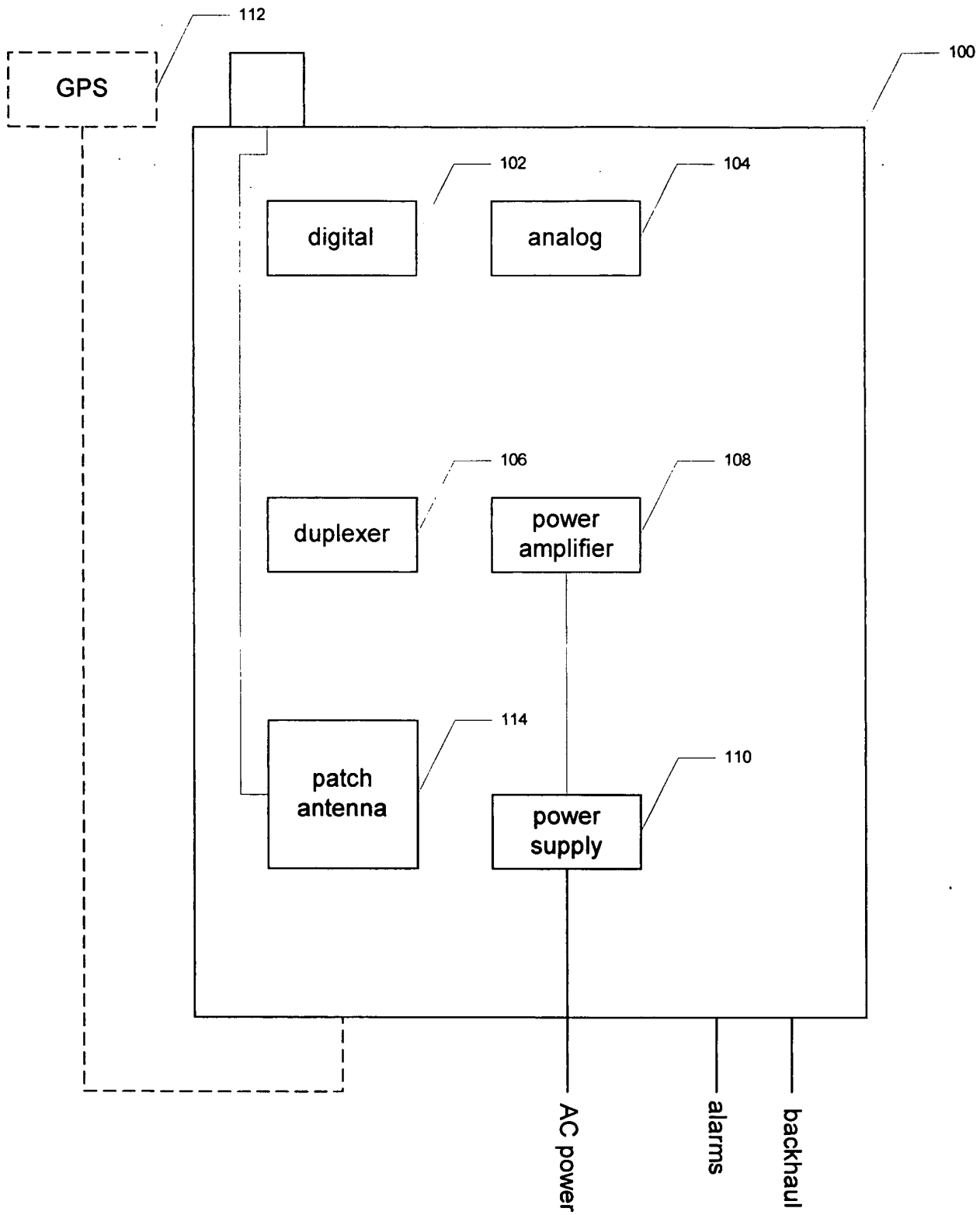


any other suitable means for providing a signal to the antenna, such as a GPS receiver, a clock, or a timer, or any combination thereof.

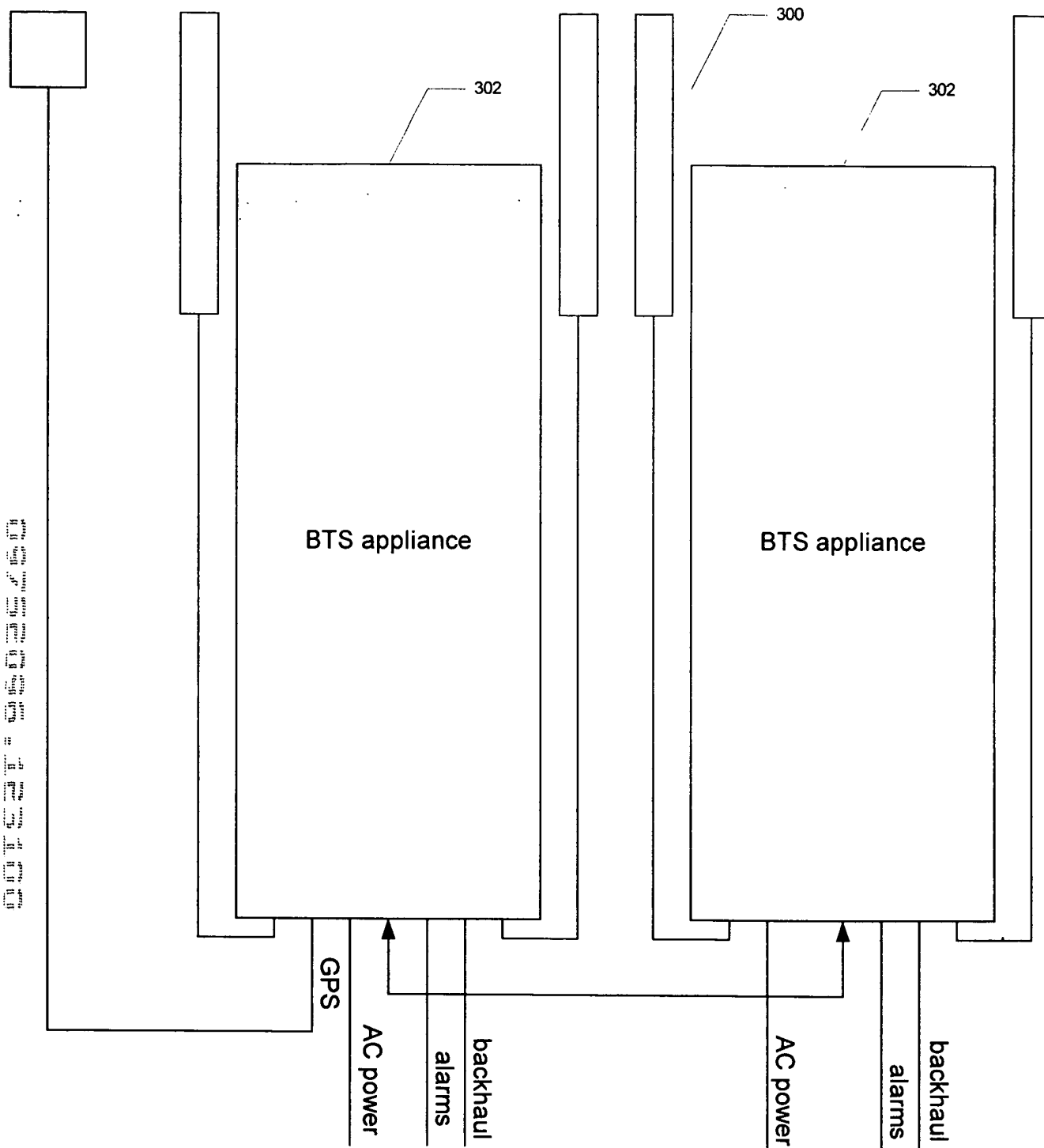


**FIG. 1**

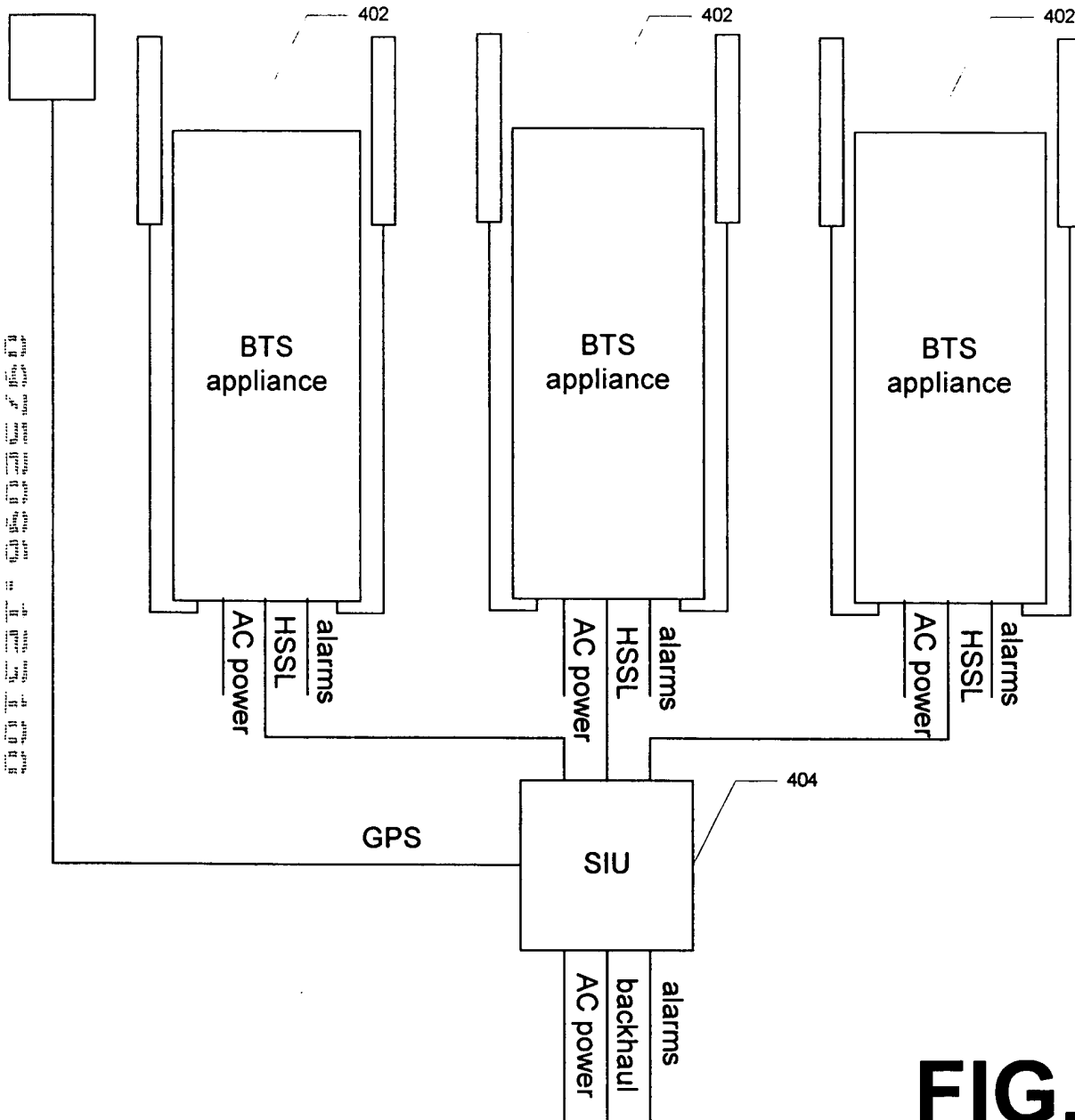
FIG. 2 is a block diagram of a system 100. The system 100 includes a GPS 112, a digital block 102, an analog block 104, a duplexer 106, a power amplifier 108, a patch antenna 114, and a power supply 110. The GPS 112 is connected to the digital block 102. The digital block 102 is connected to the analog block 104. The analog block 104 is connected to the duplexer 106. The duplexer 106 is connected to the patch antenna 114. The power amplifier 108 is connected to the duplexer 106. The power supply 110 is connected to the power amplifier 108. The system 100 is also connected to AC power, alarms, and backhaul.



**FIG. 2**



**FIG. 3**



**FIG. 4**

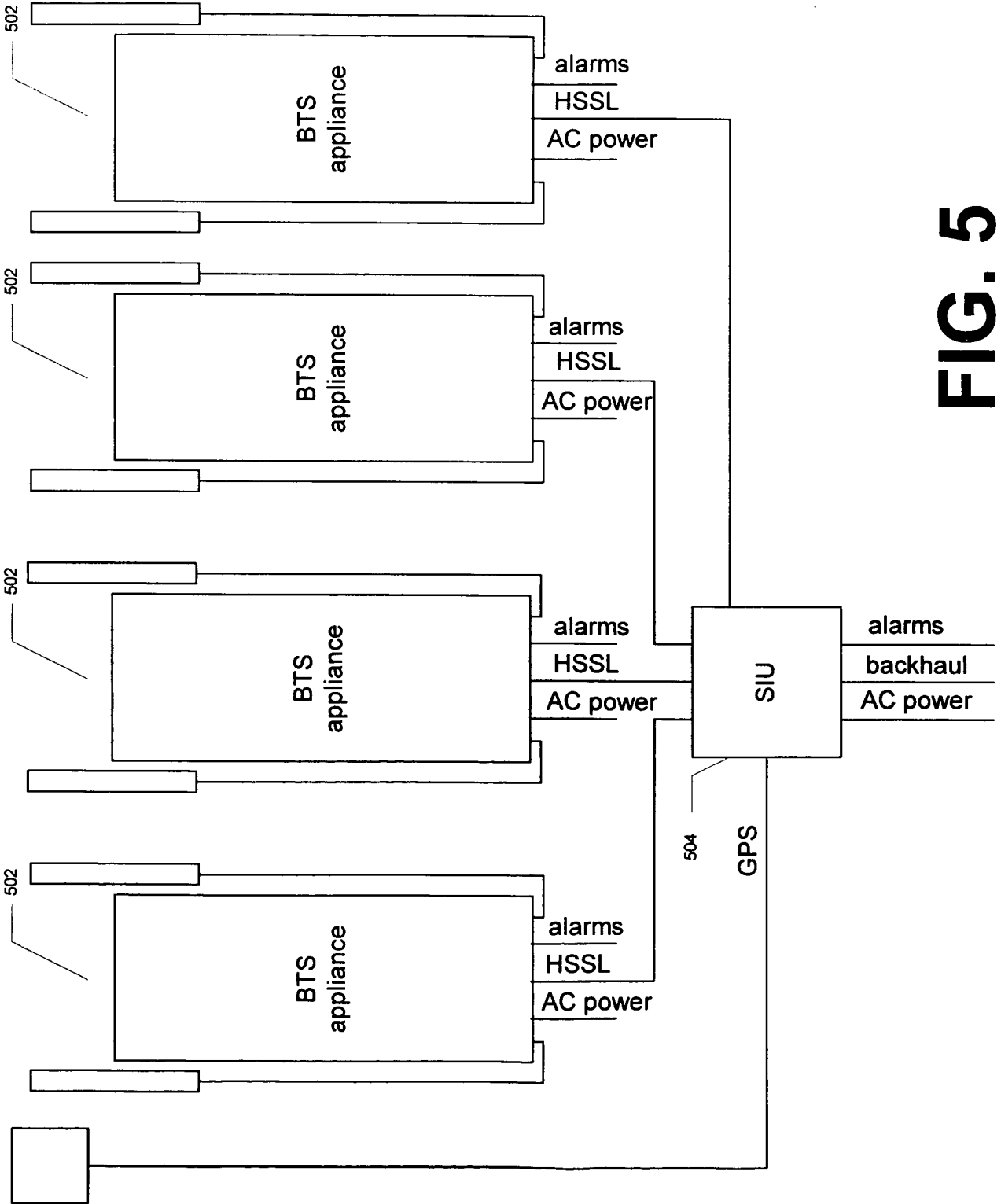


FIG. 5



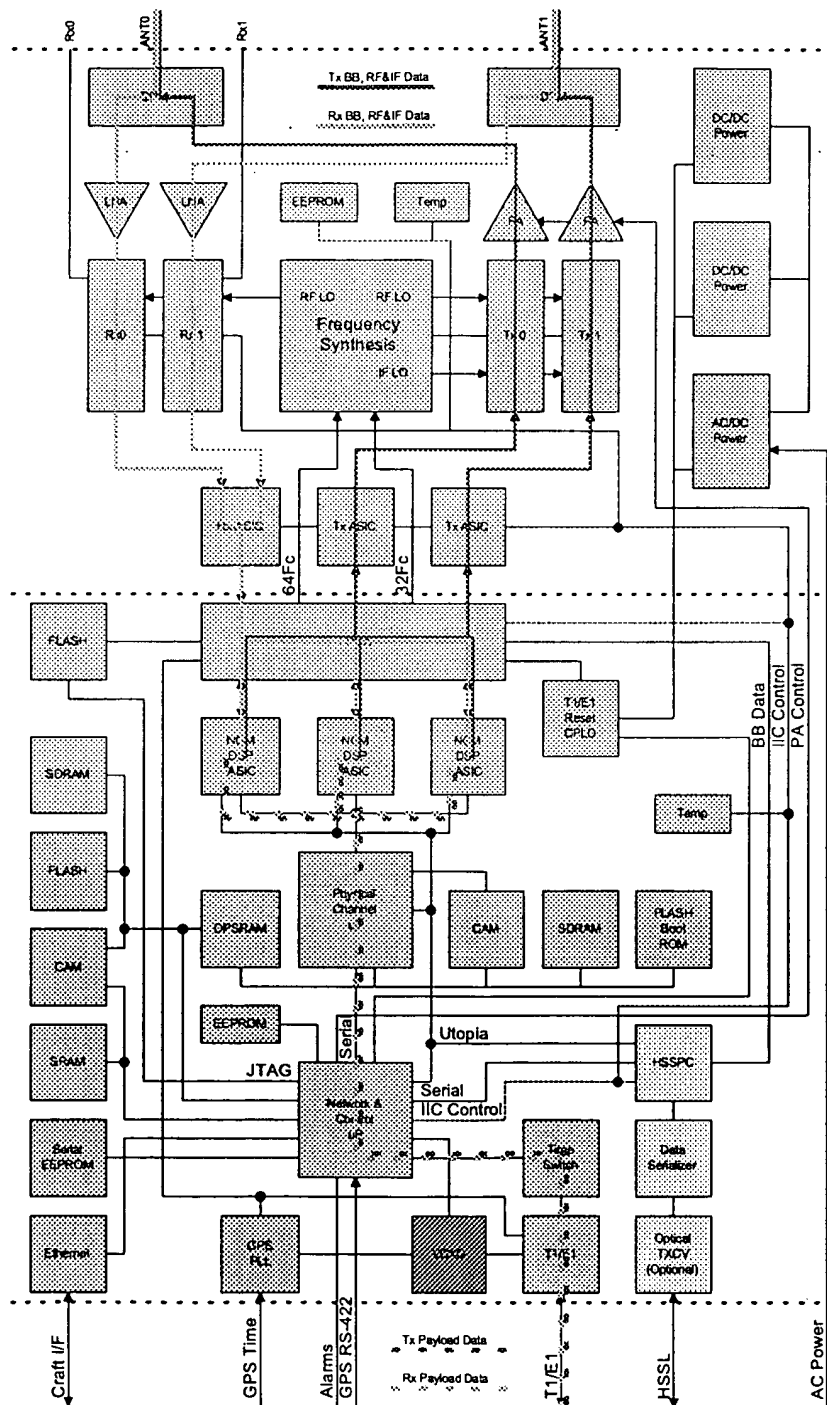
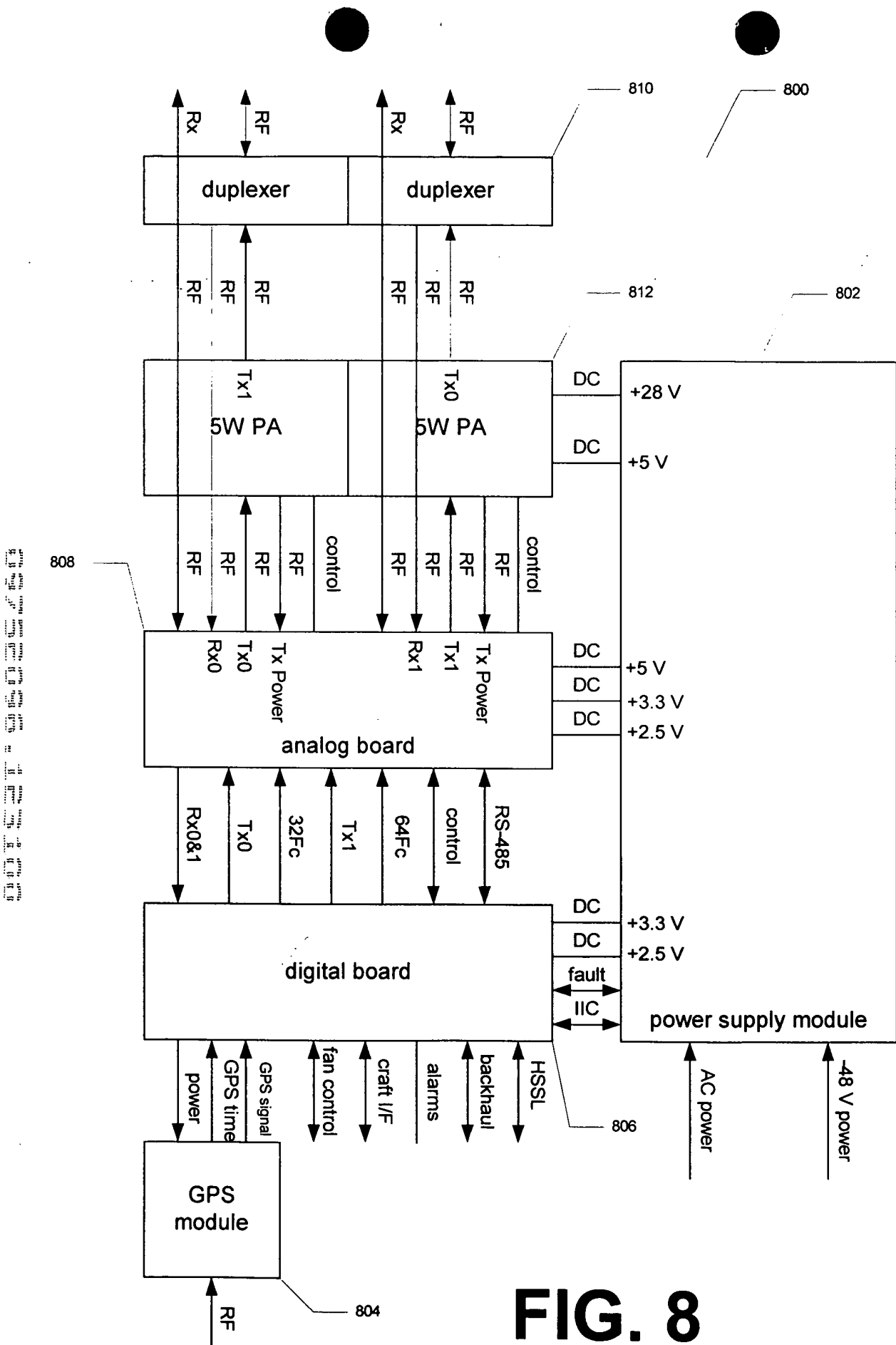
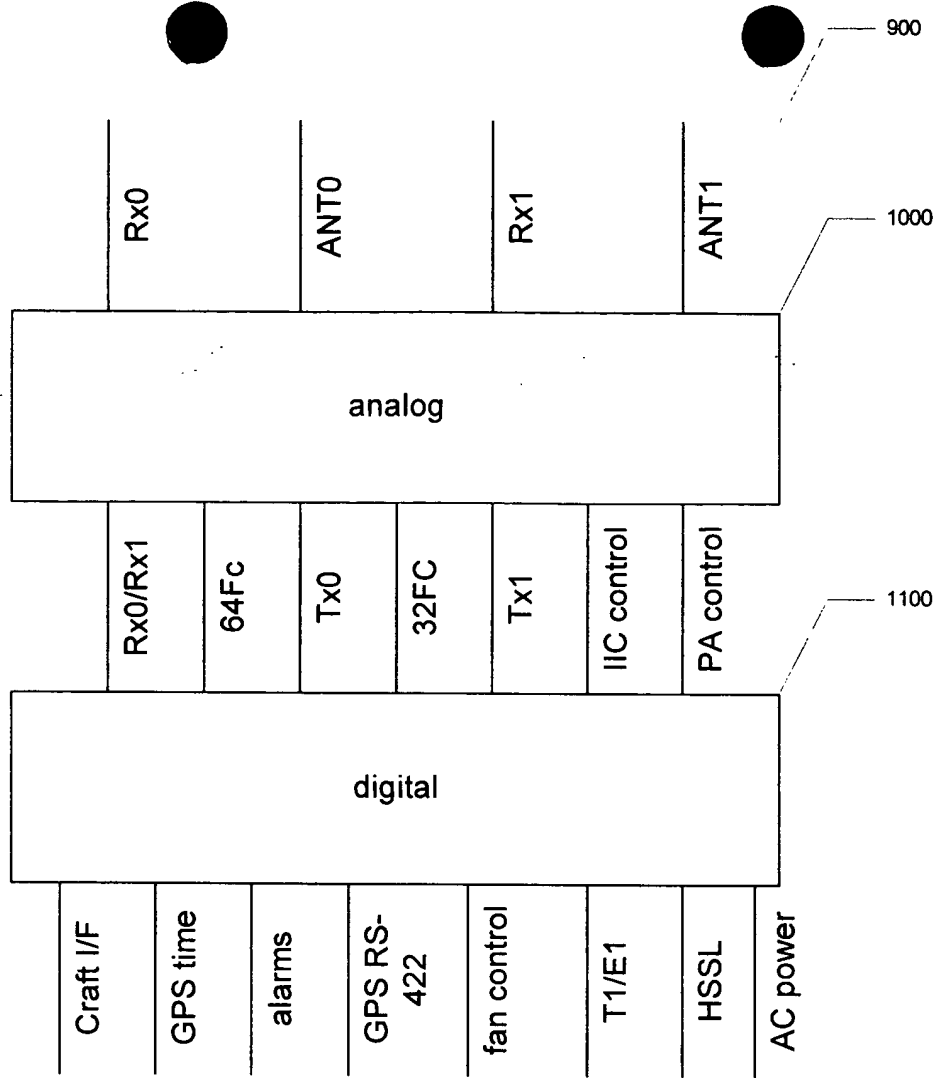


FIG. 7



**FIG. 8**





**FIG. 9**

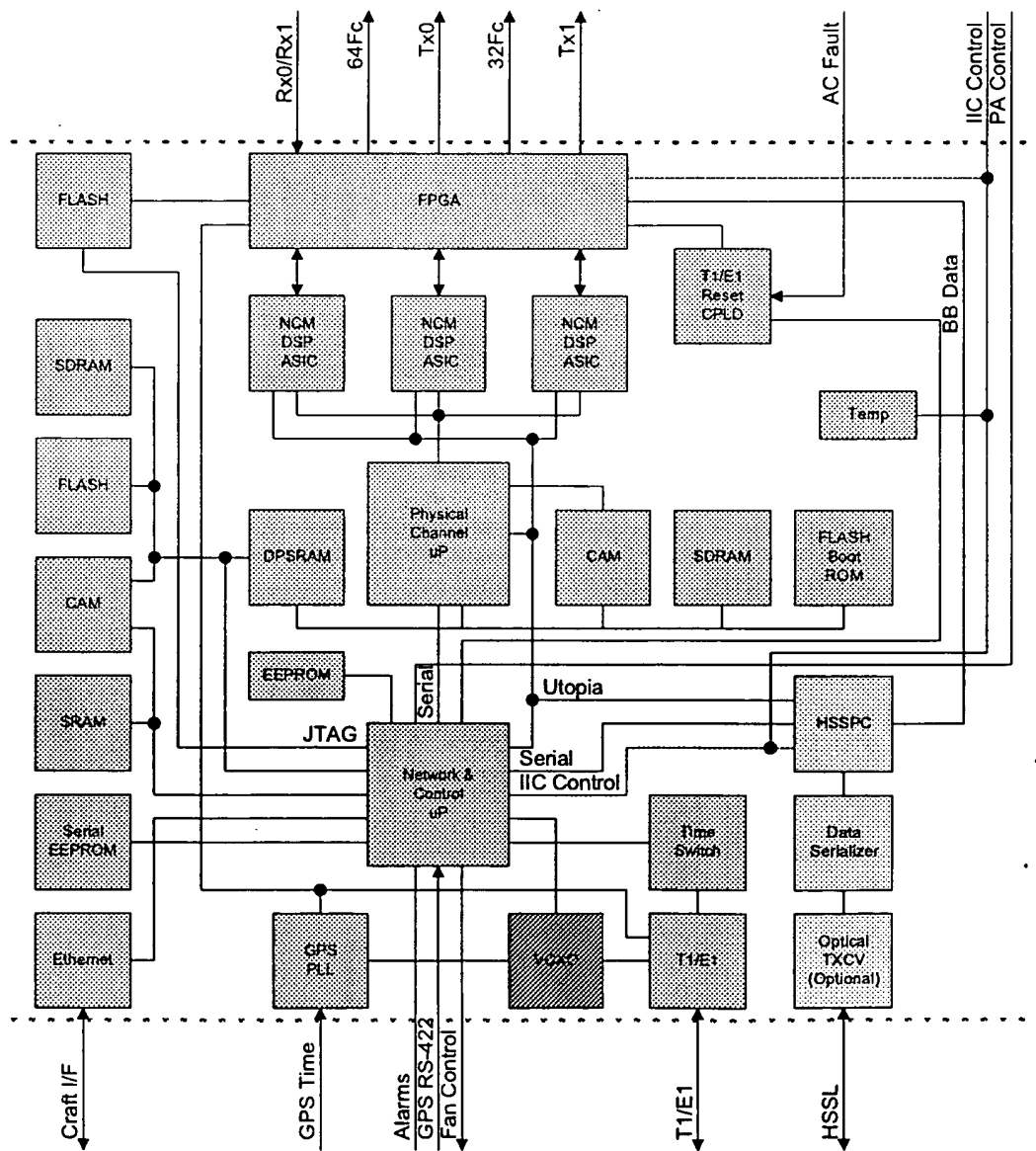
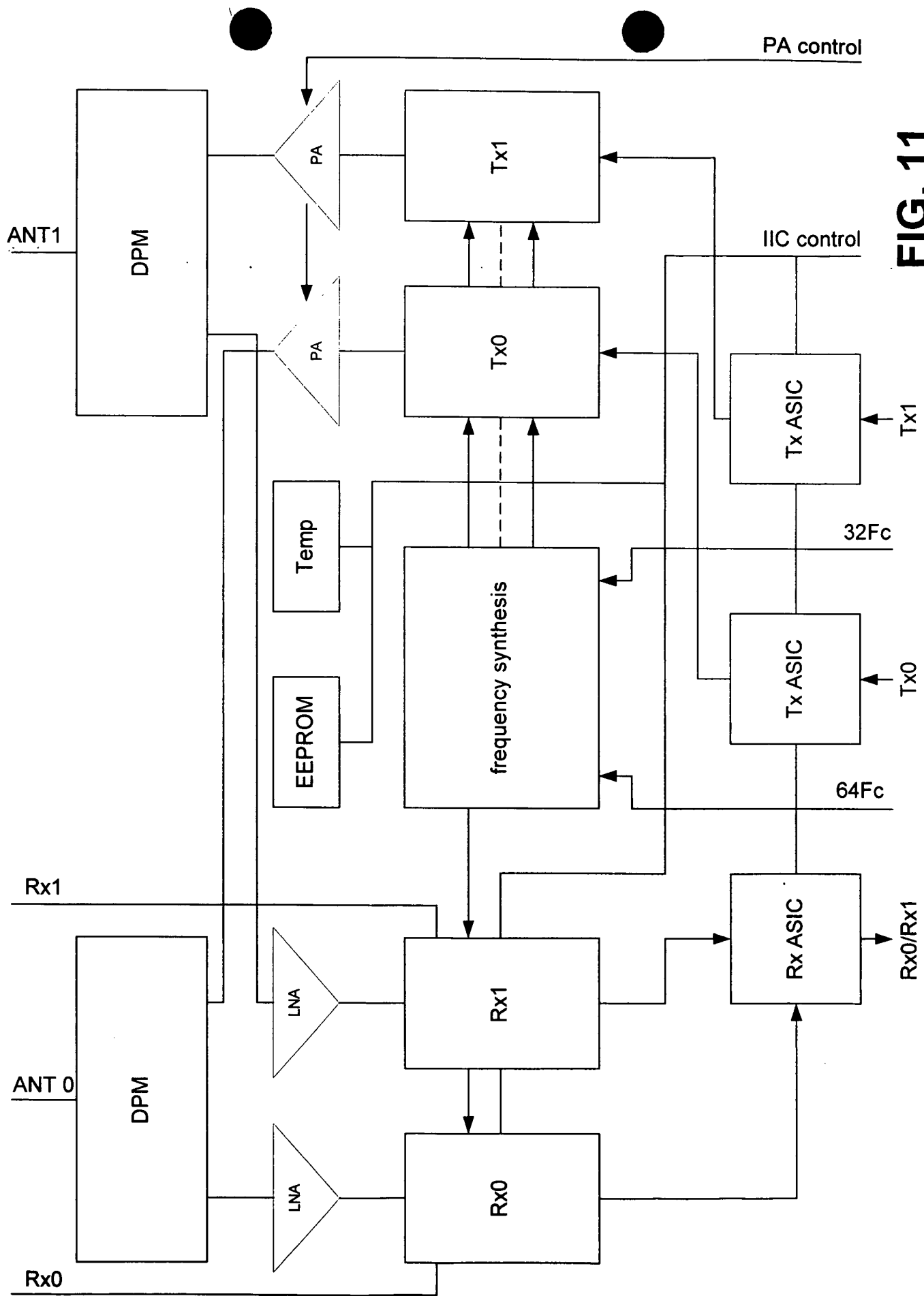


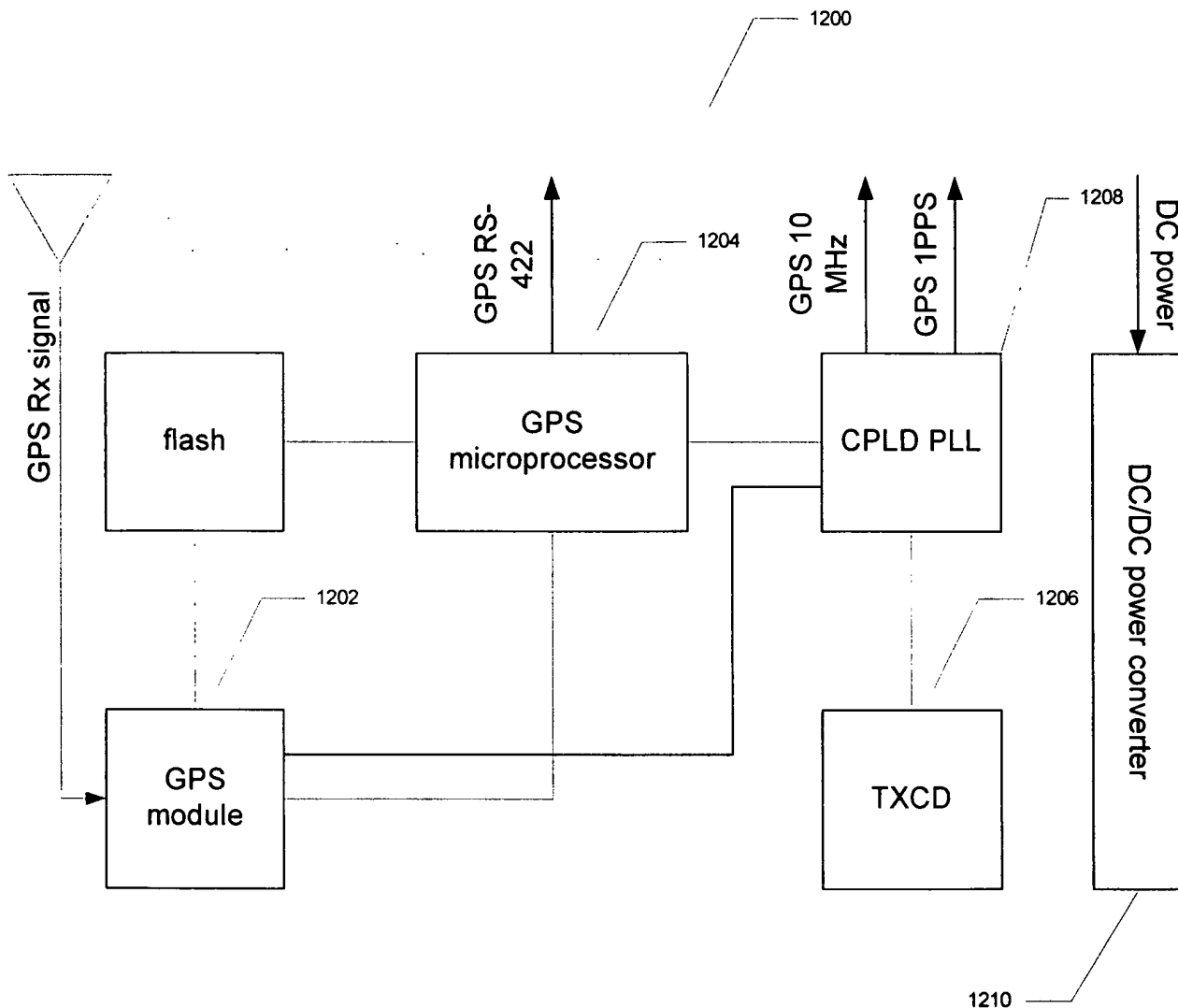
FIG. 10



**FIG. 11**

FIG. 11 is a block diagram of a dual-band transceiver system. The system includes two parallel channels for Tx0 and Tx1, and Rx0 and Rx1. The system is controlled via PA control and IIC control lines. The Tx path includes a frequency synthesizer, Tx ASICs, and PA blocks. The Rx path includes LNA blocks, Rx ASICs, and an antenna. The system also includes EEPROM and Temp sensors connected to the frequency synthesizer.

FIG. 12 is a block diagram of a GPS system 1200. The system 1200 includes a GPS module 1202, a flash memory 1204, a GPS microprocessor 1206, a CPLD PLL 1208, a TXCD 1210, and a DC/DC power converter 1212. The GPS module 1202 receives a GPS Rx signal 1201 and outputs a GPS RS-422 signal 1203 to the GPS microprocessor 1206. The flash memory 1204 is connected to the GPS microprocessor 1206. The GPS microprocessor 1206 is connected to the CPLD PLL 1208, which outputs a GPS 10 MHz signal 1209 and a GPS 1 PPS signal 1211. The GPS microprocessor 1206 is also connected to the TXCD 1210. The TXCD 1210 is connected to the DC/DC power converter 1212, which provides DC power 1213 to the system 1200.



**FIG. 12**

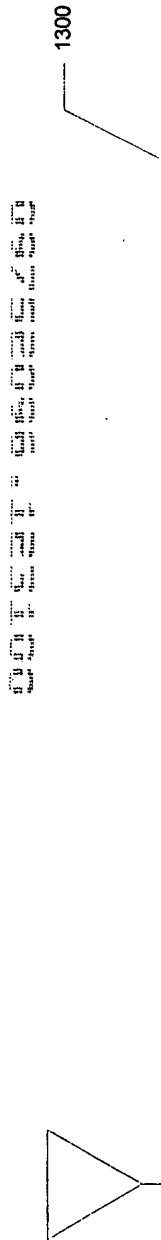
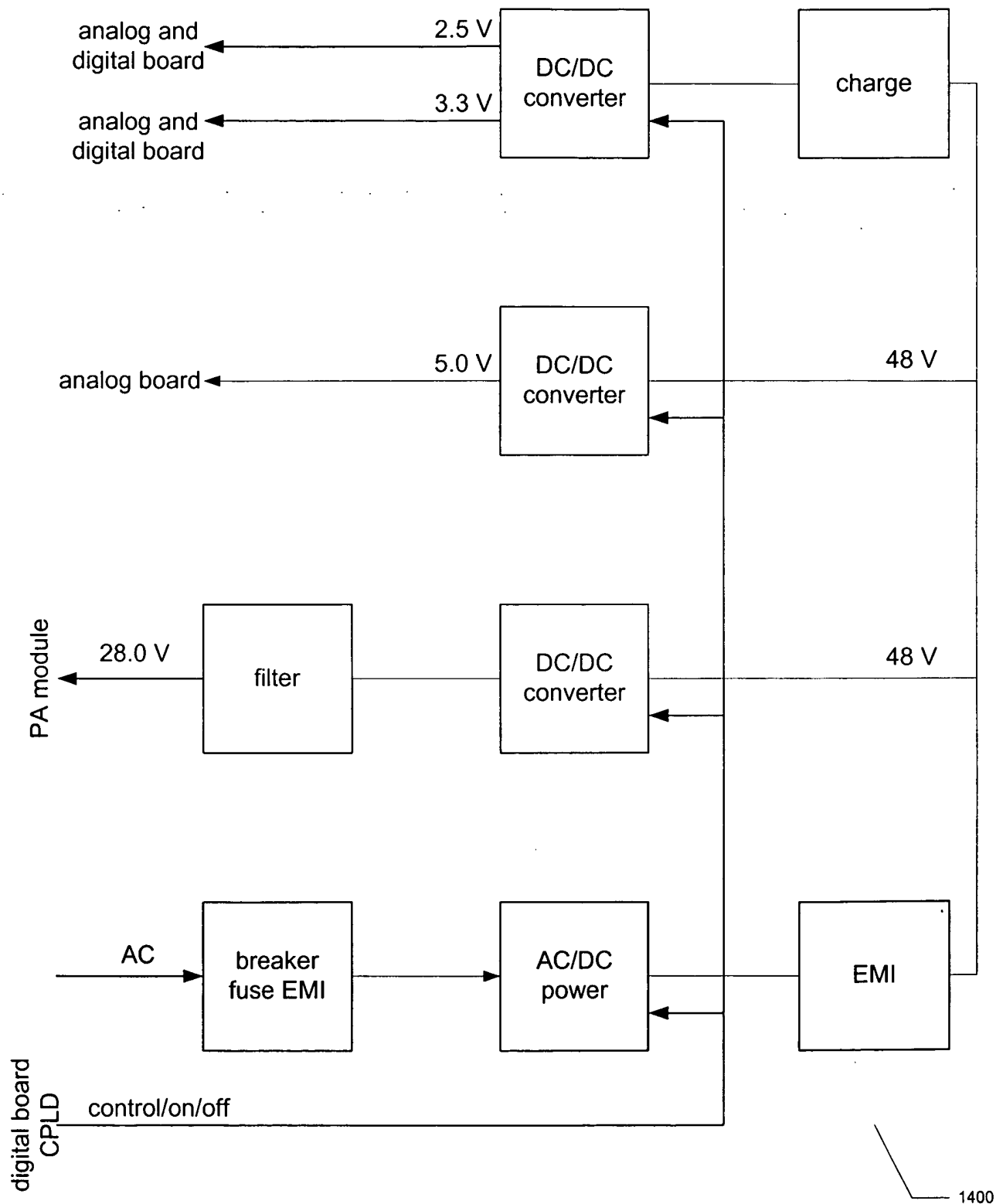


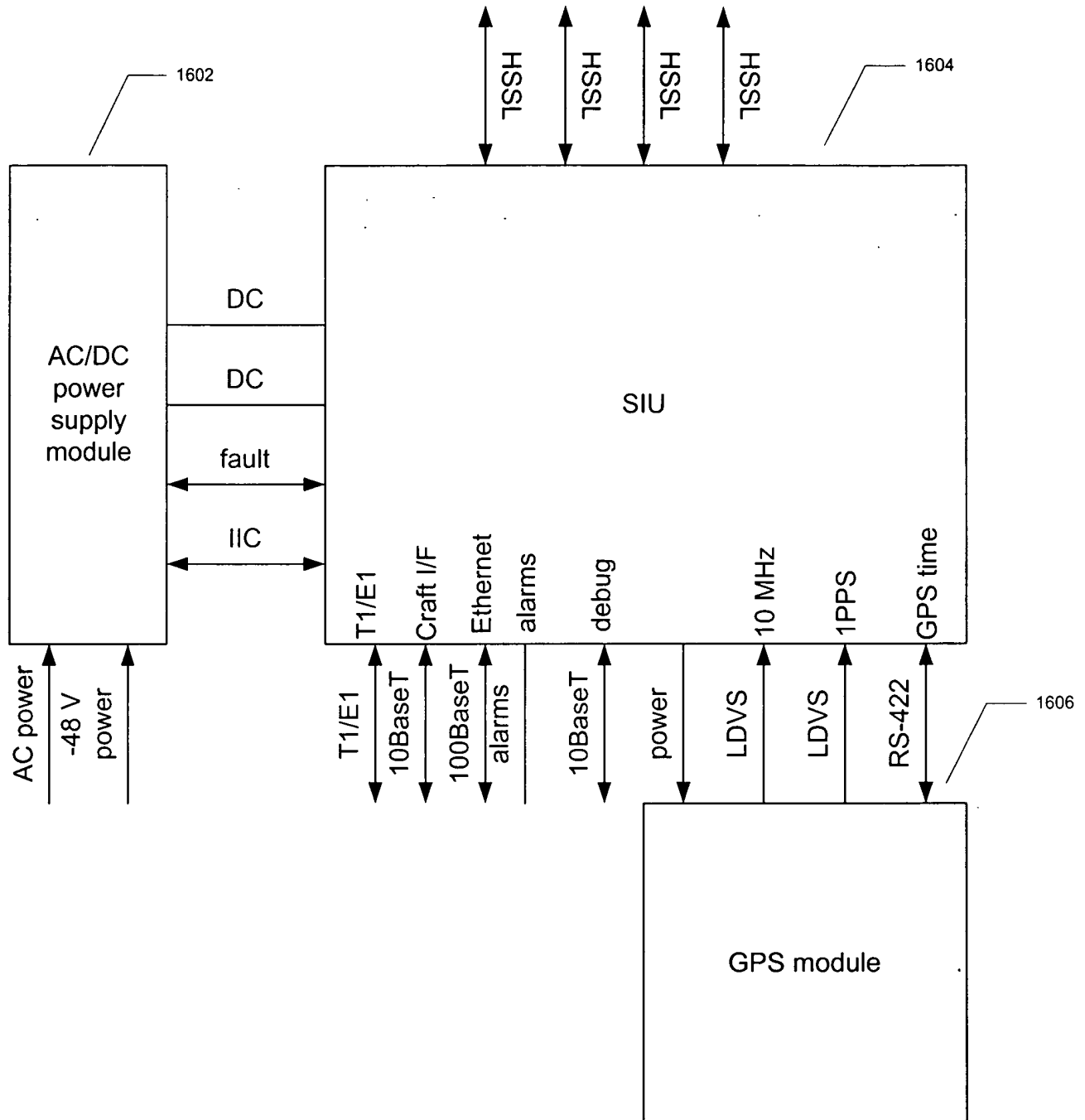
FIG. 13

FIG. 14 is a block diagram of a power supply system 1400. The system includes an AC input, a breaker fuse EMI, an AC/DC power converter, a charge controller, and three DC/DC converters. The AC input is connected to the breaker fuse EMI, which is connected to the AC/DC power converter. The AC/DC power converter is connected to the charge controller. The charge controller is connected to the three DC/DC converters. The DC/DC converters are connected to the analog and digital board, the analog board, and the PA module. The digital board CPLD is connected to the AC/DC power converter and the charge controller.



**FIG. 14**





**FIG. 16**



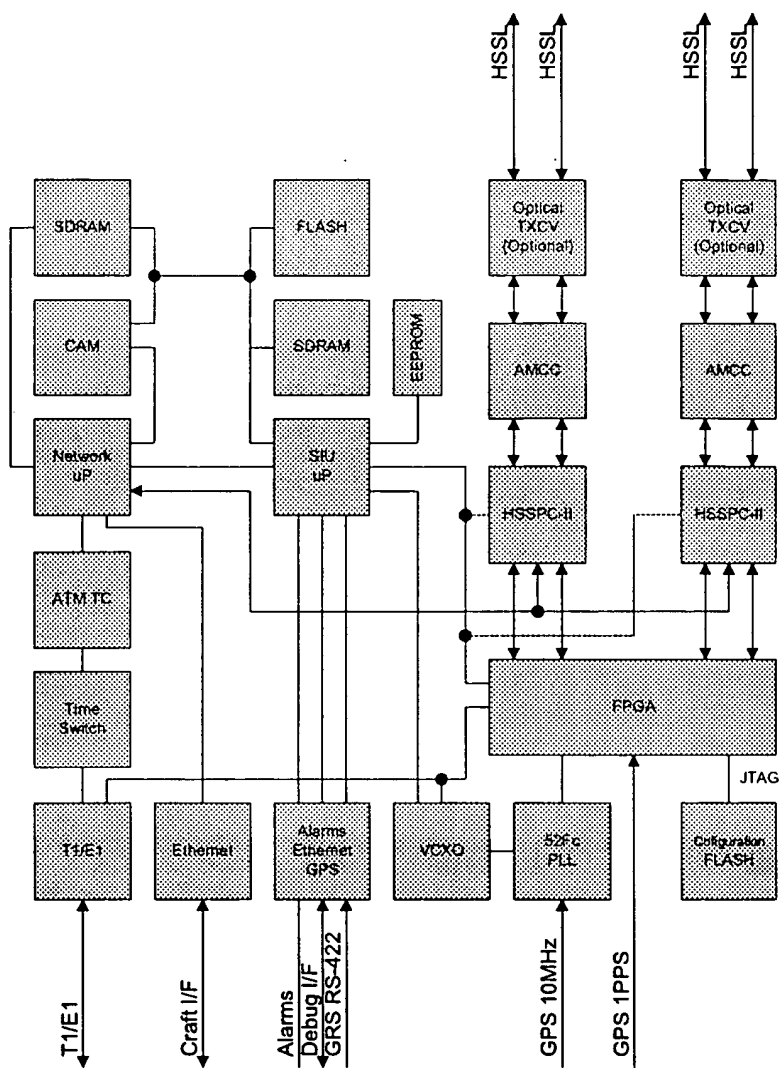
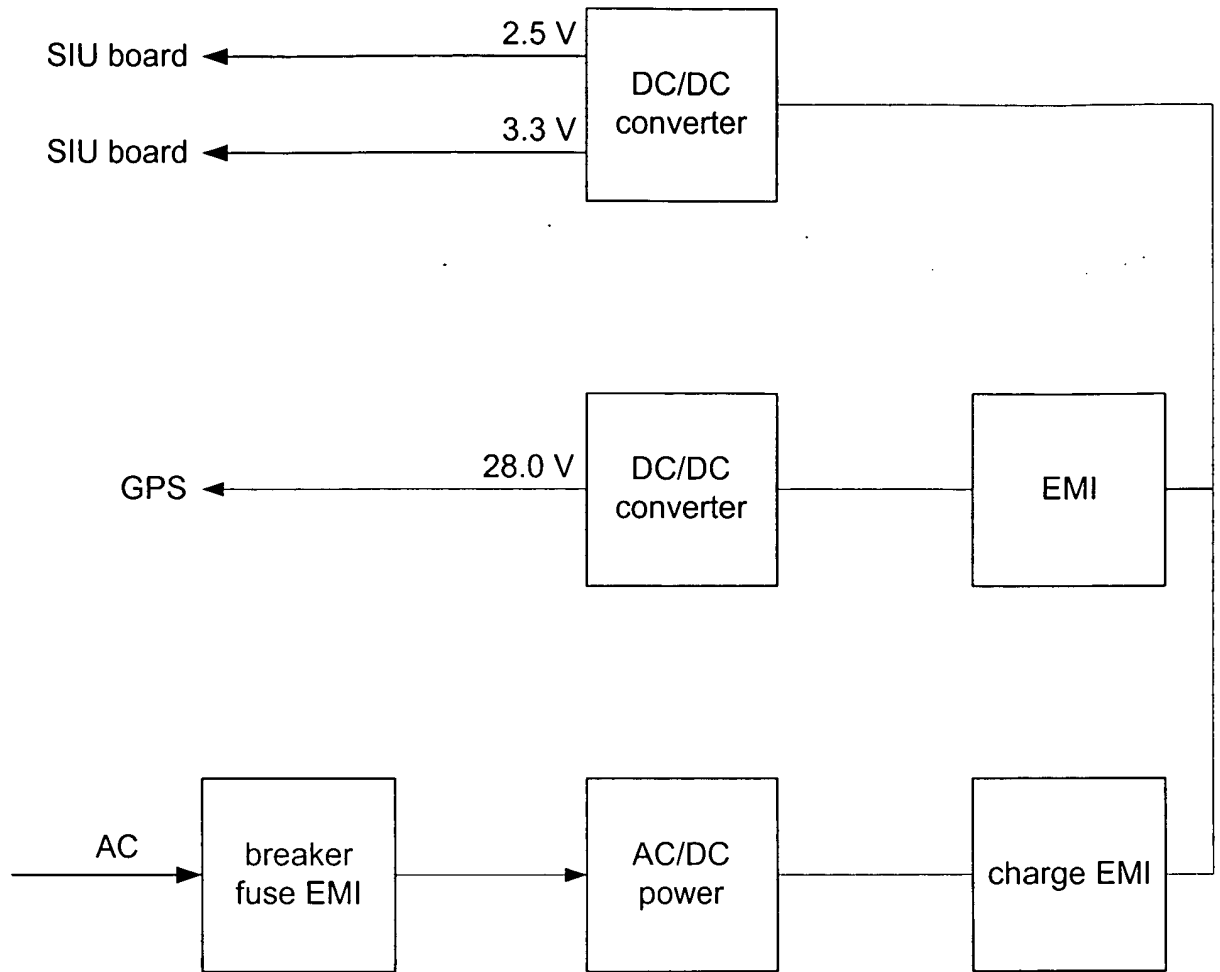
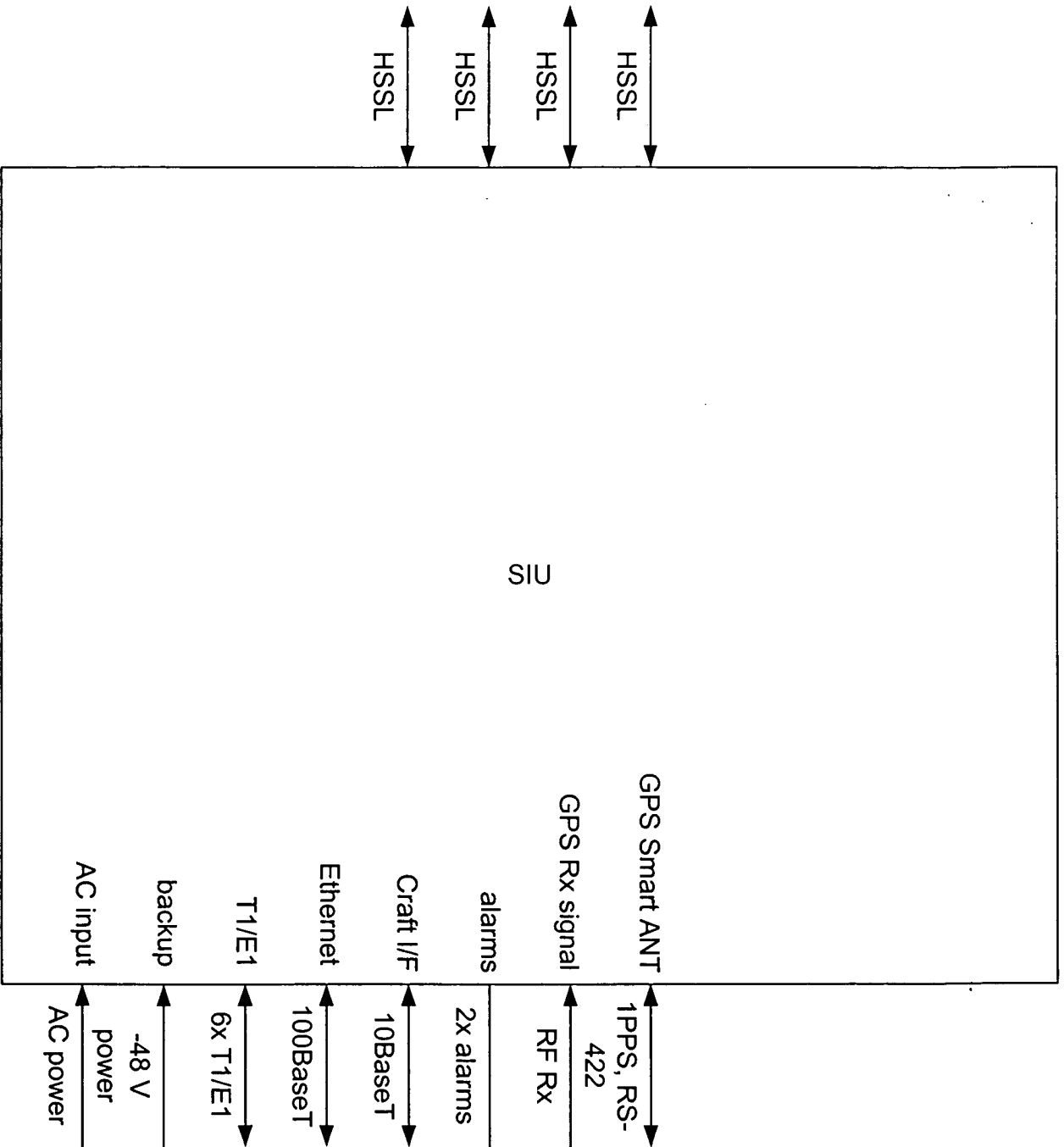


FIG. 17



1602

**FIG. 18**



**FIG. 19**

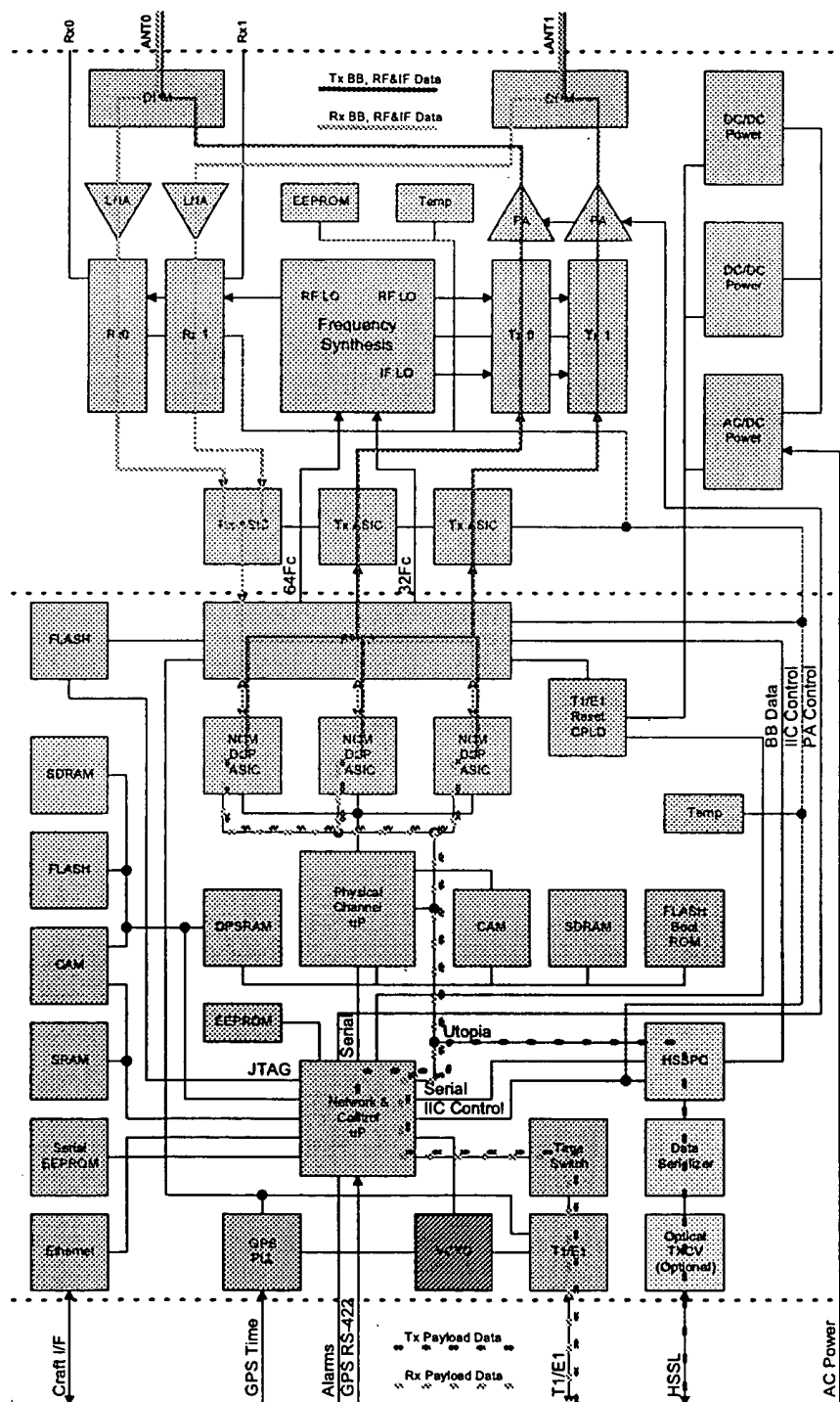


FIG. 20

FIG. 21 is a block diagram of a system architecture. The diagram is divided into three main sections: a top section for RF and baseband processing, a middle section for system control and data processing, and a bottom section for external interfaces and power management.

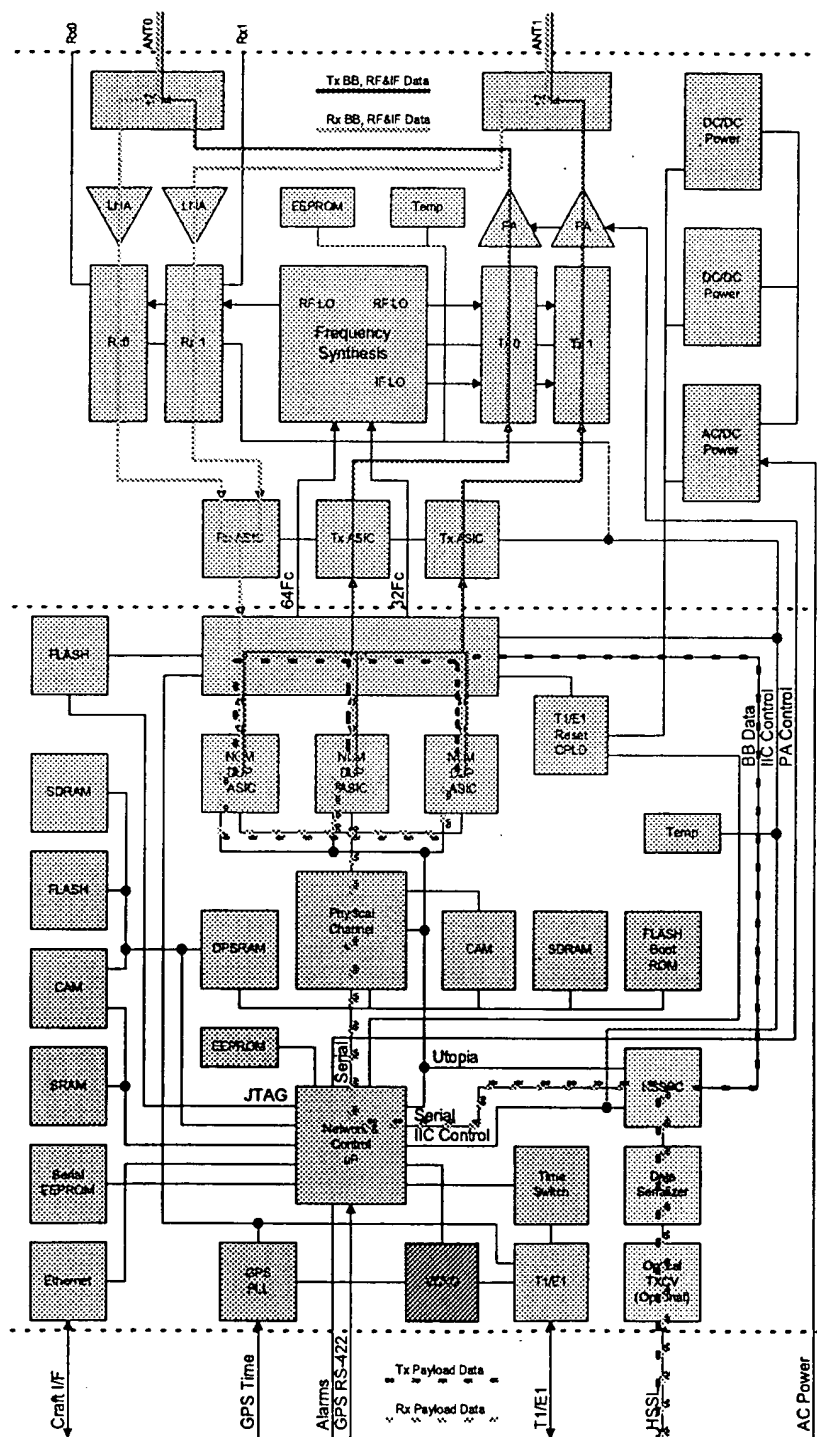
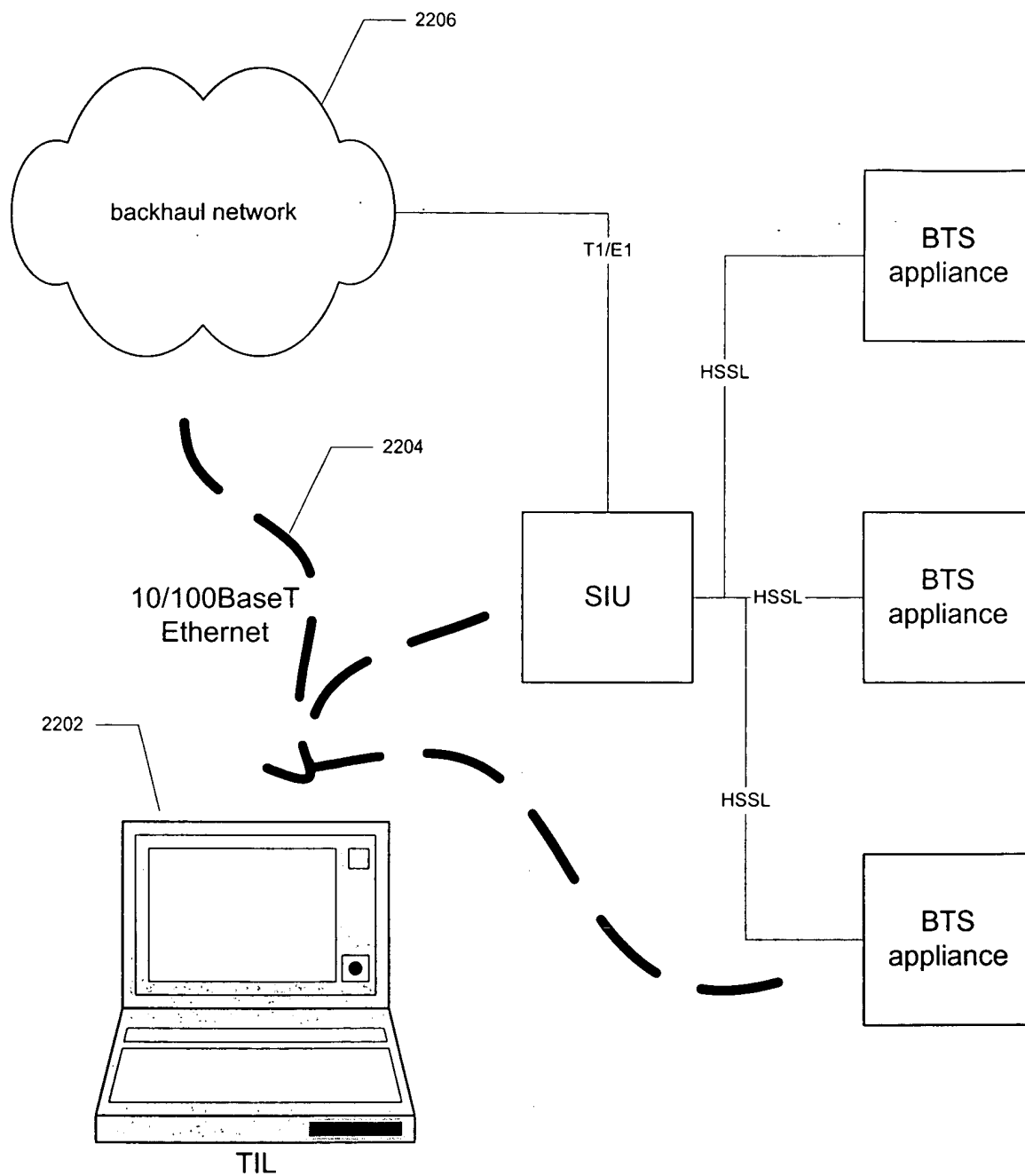


FIG. 21



**FIG. 22**

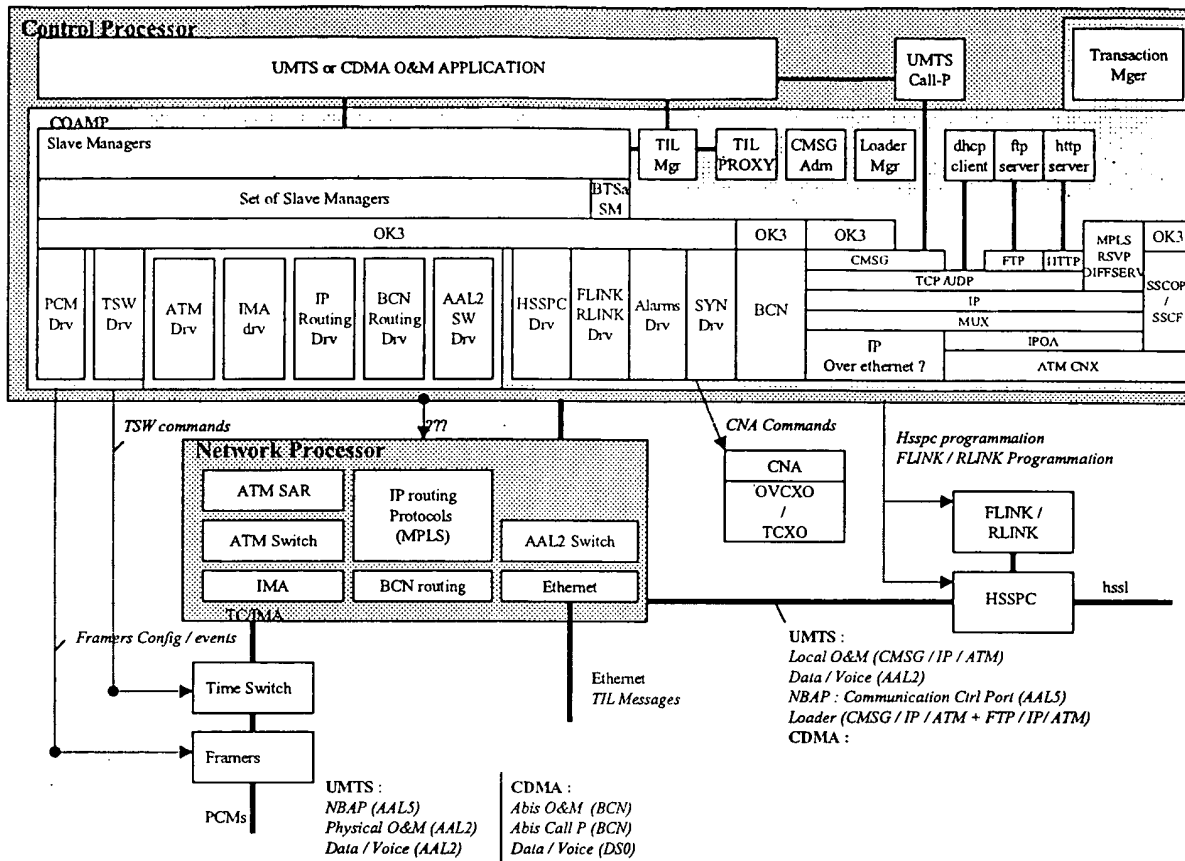


FIG. 23

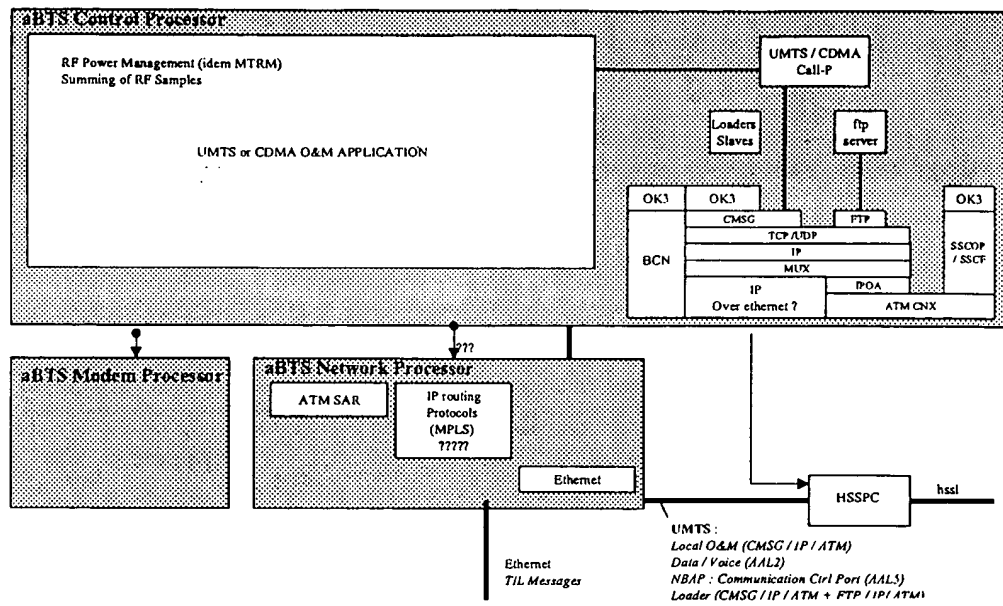


FIG. 24



2500

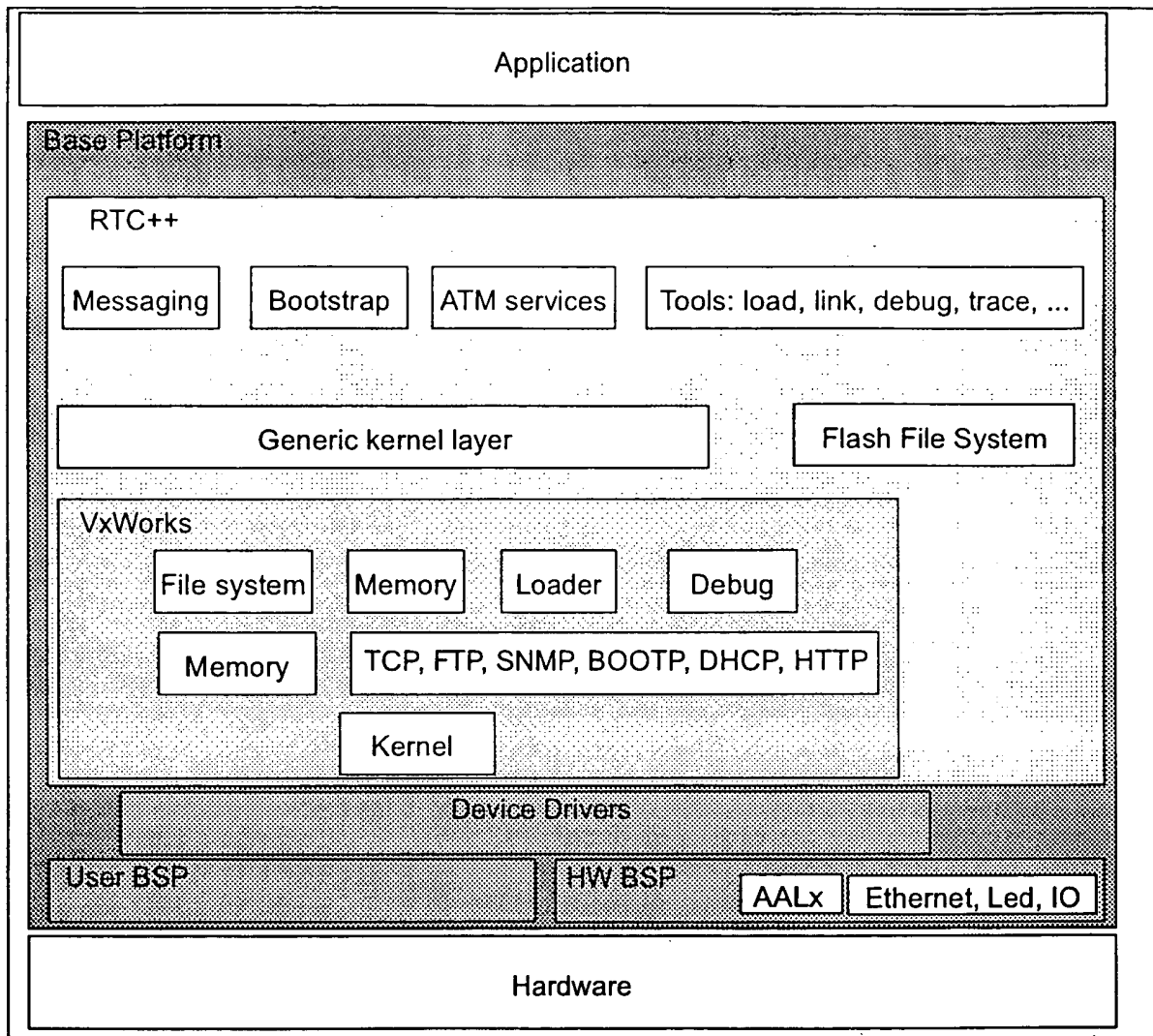


FIG. 25

2600

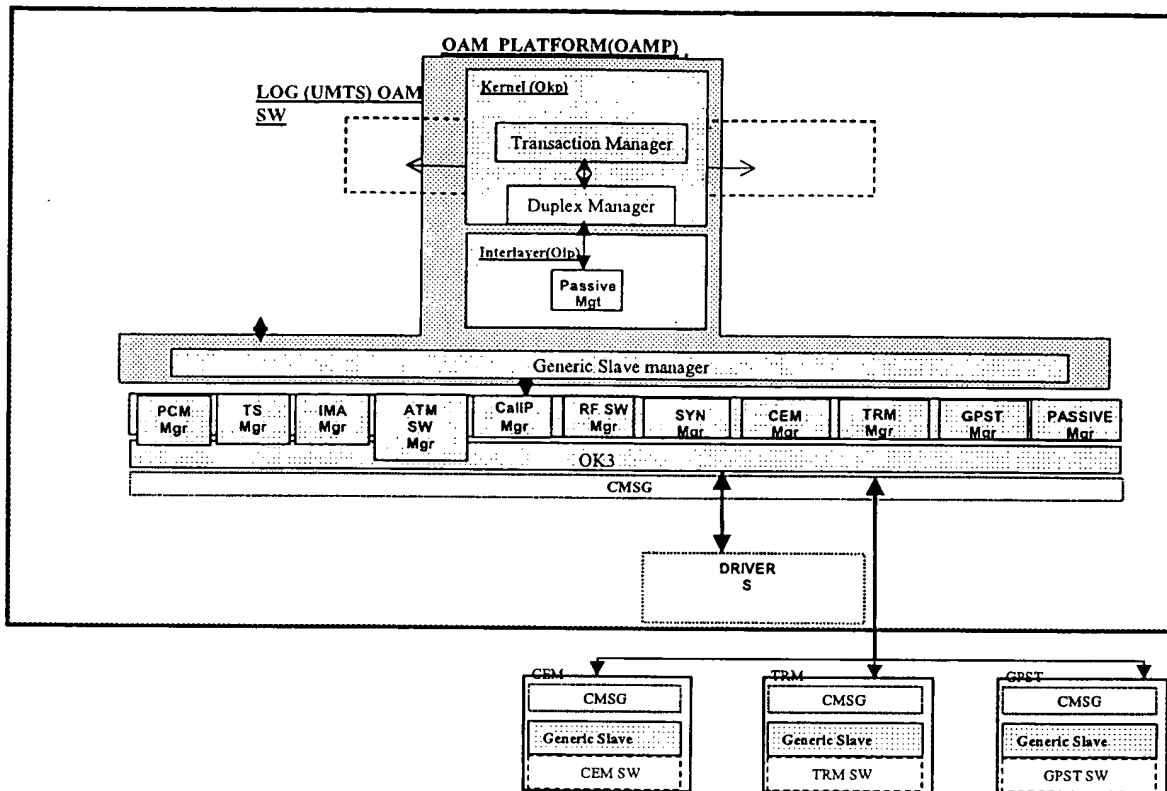


FIG. 26

2700

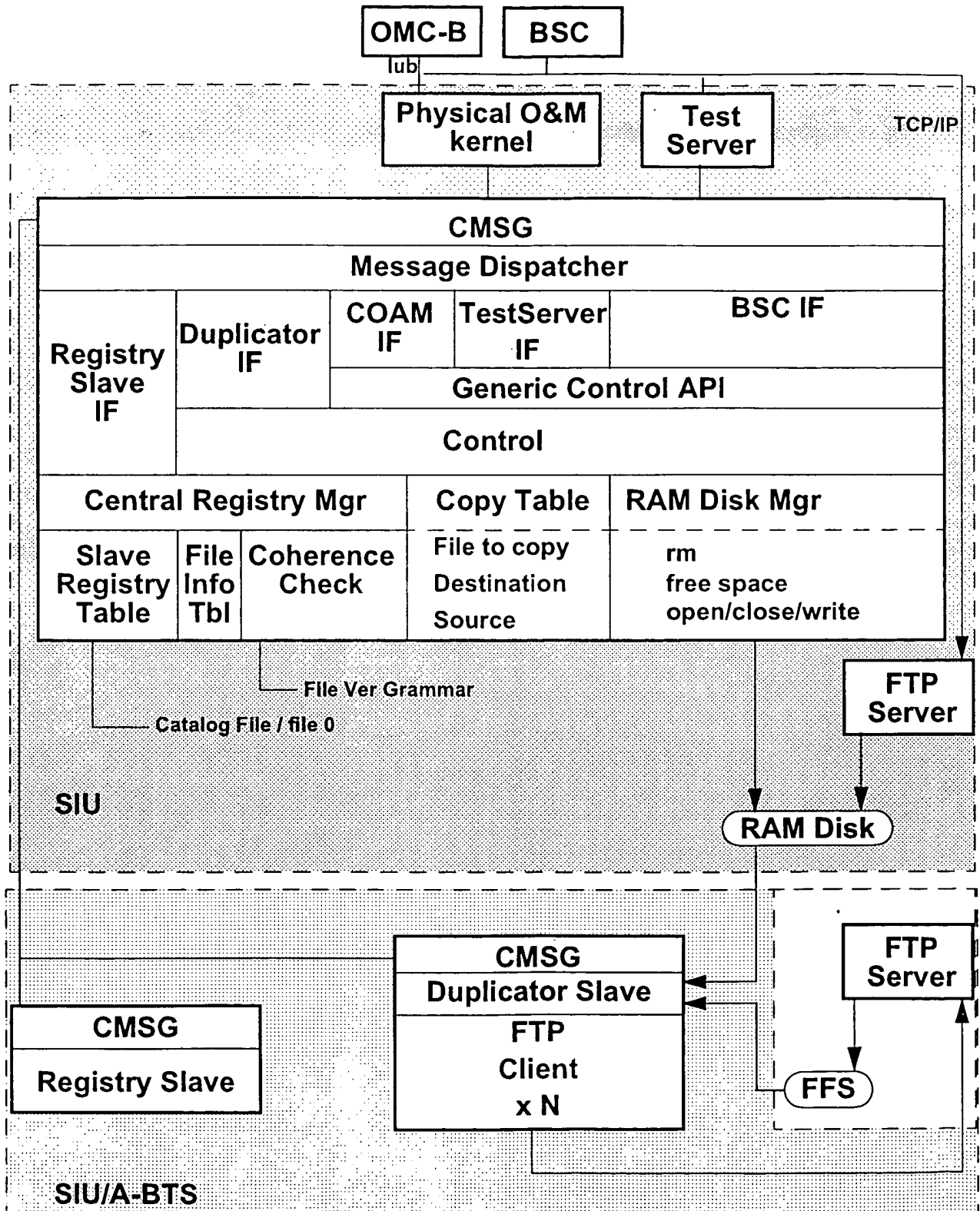


FIG. 27

2800

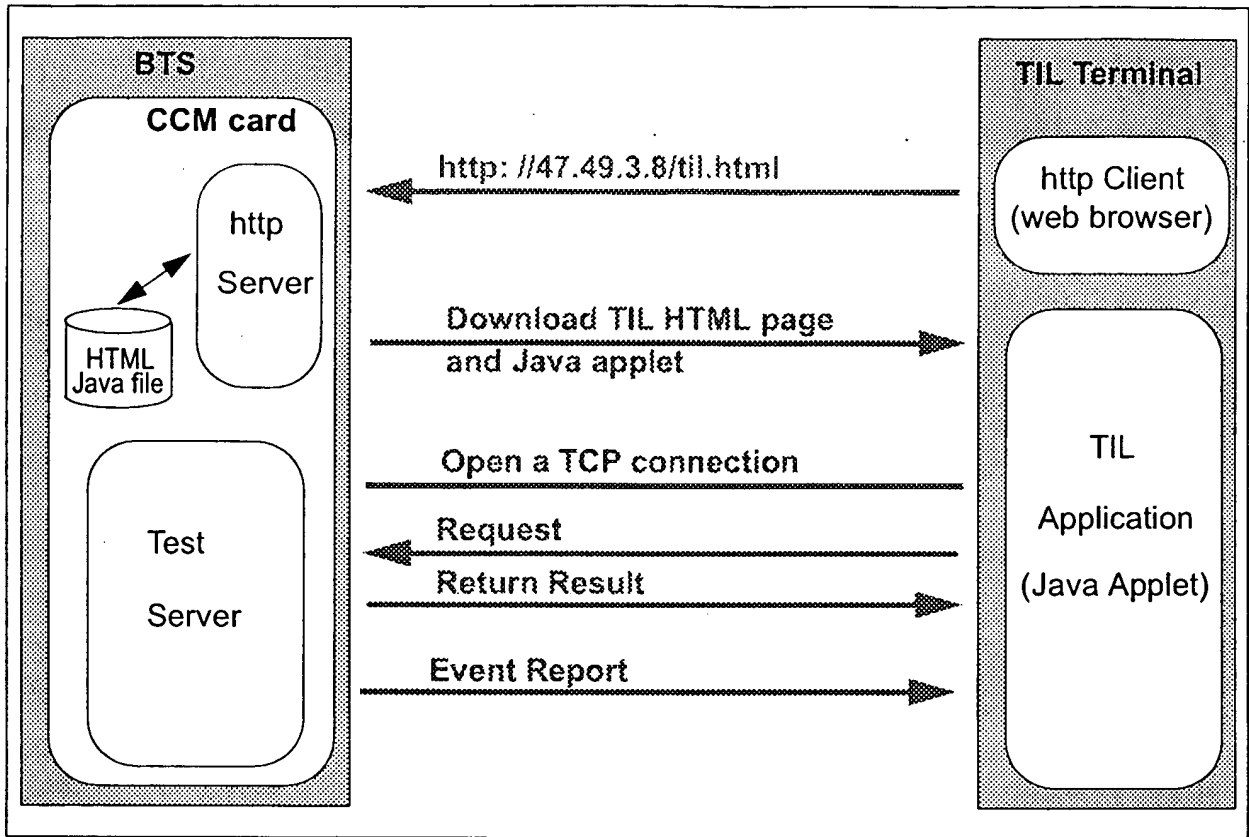


FIG. 28

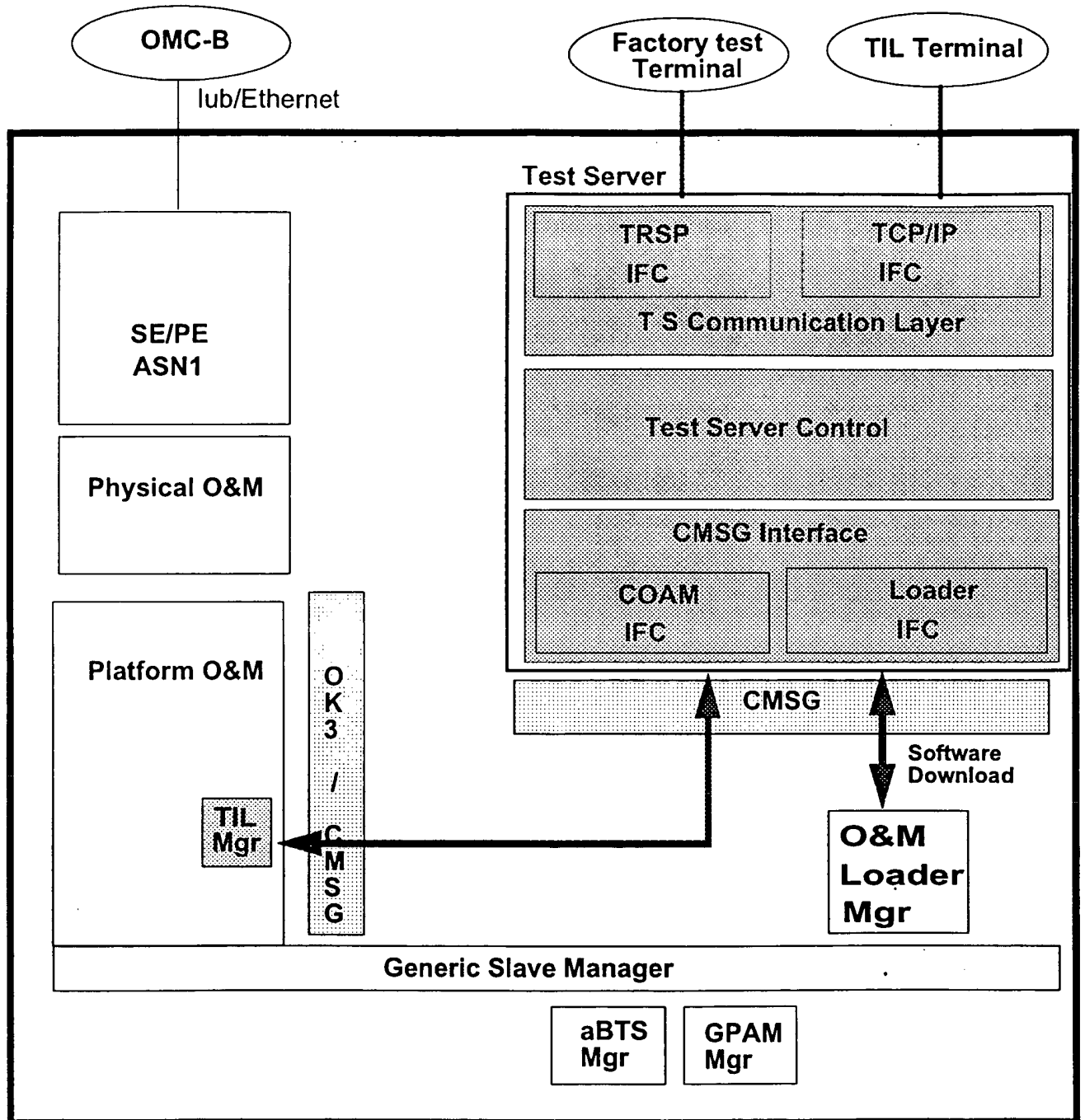
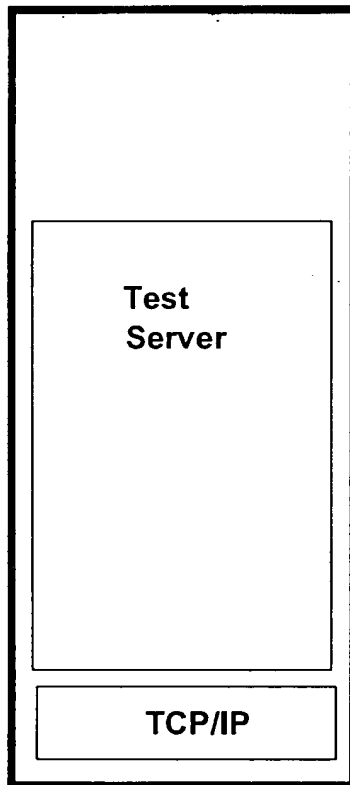
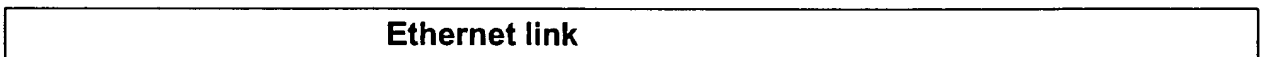
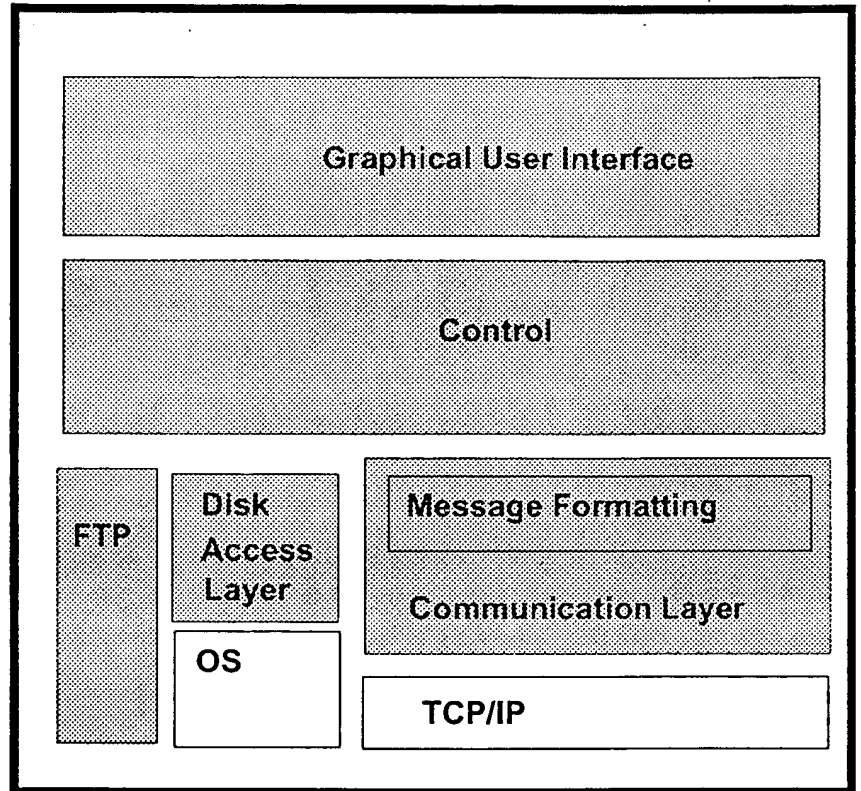


FIG. 29

SIU card



TIL Terminal



 TIL Application Layers

FIG. 30

53100

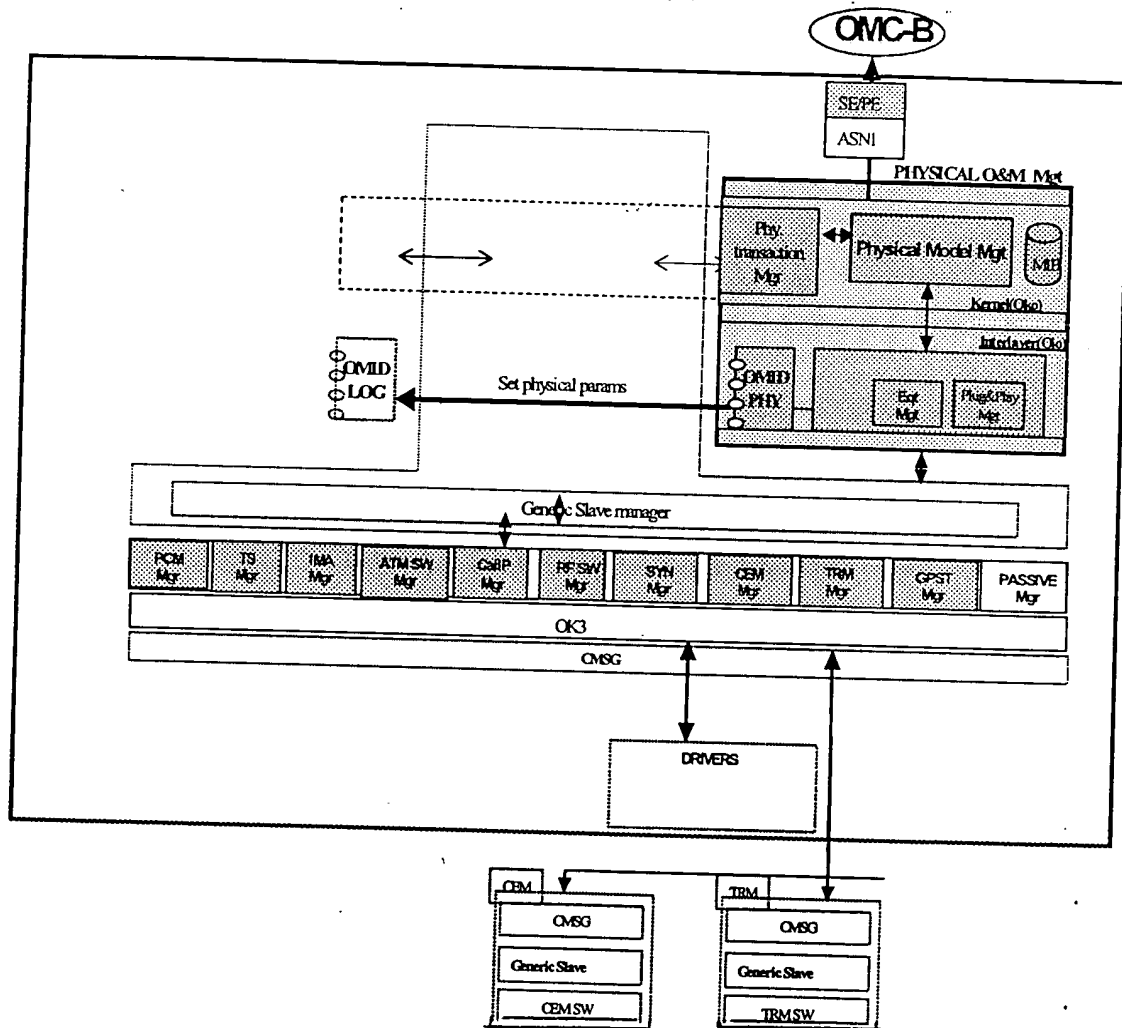


FIG. 31





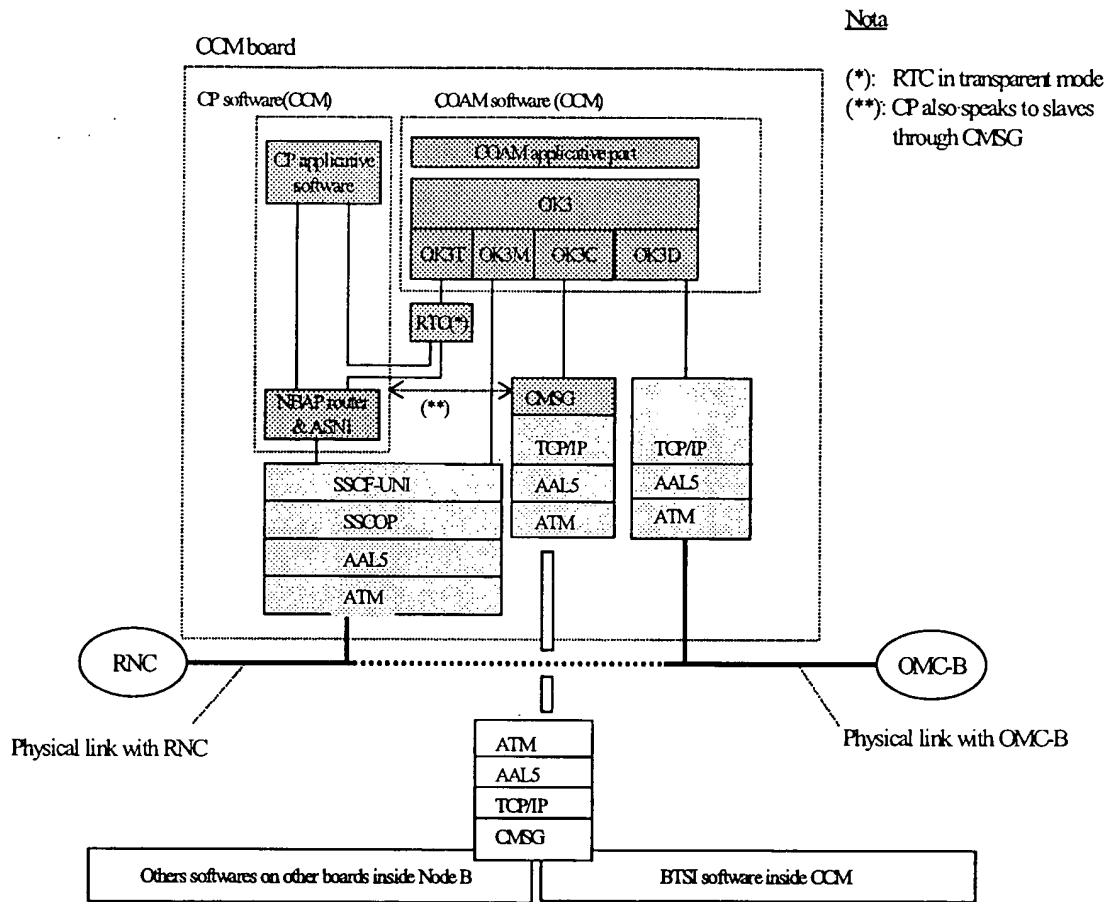


FIG. 33

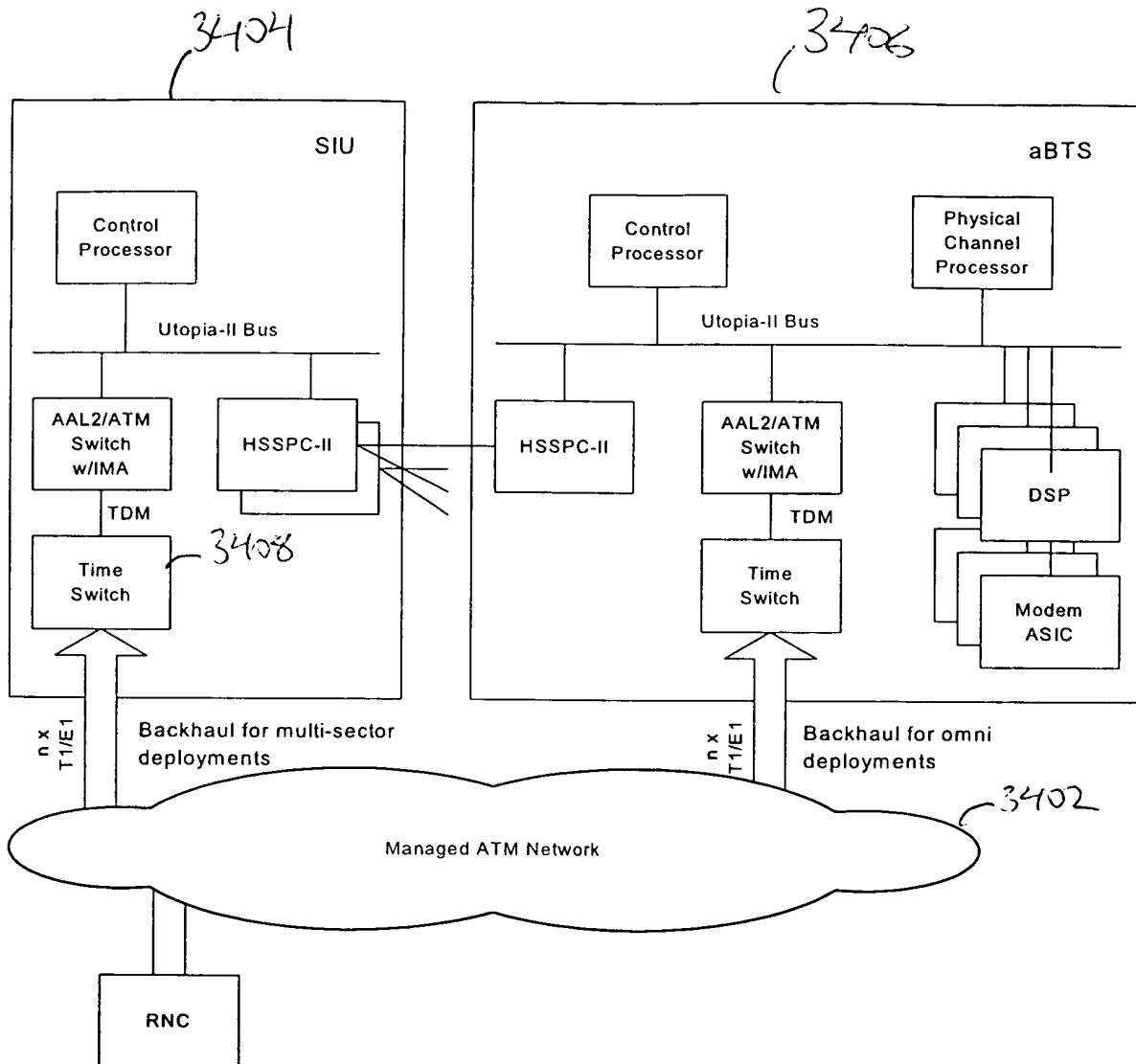


FIG. 34

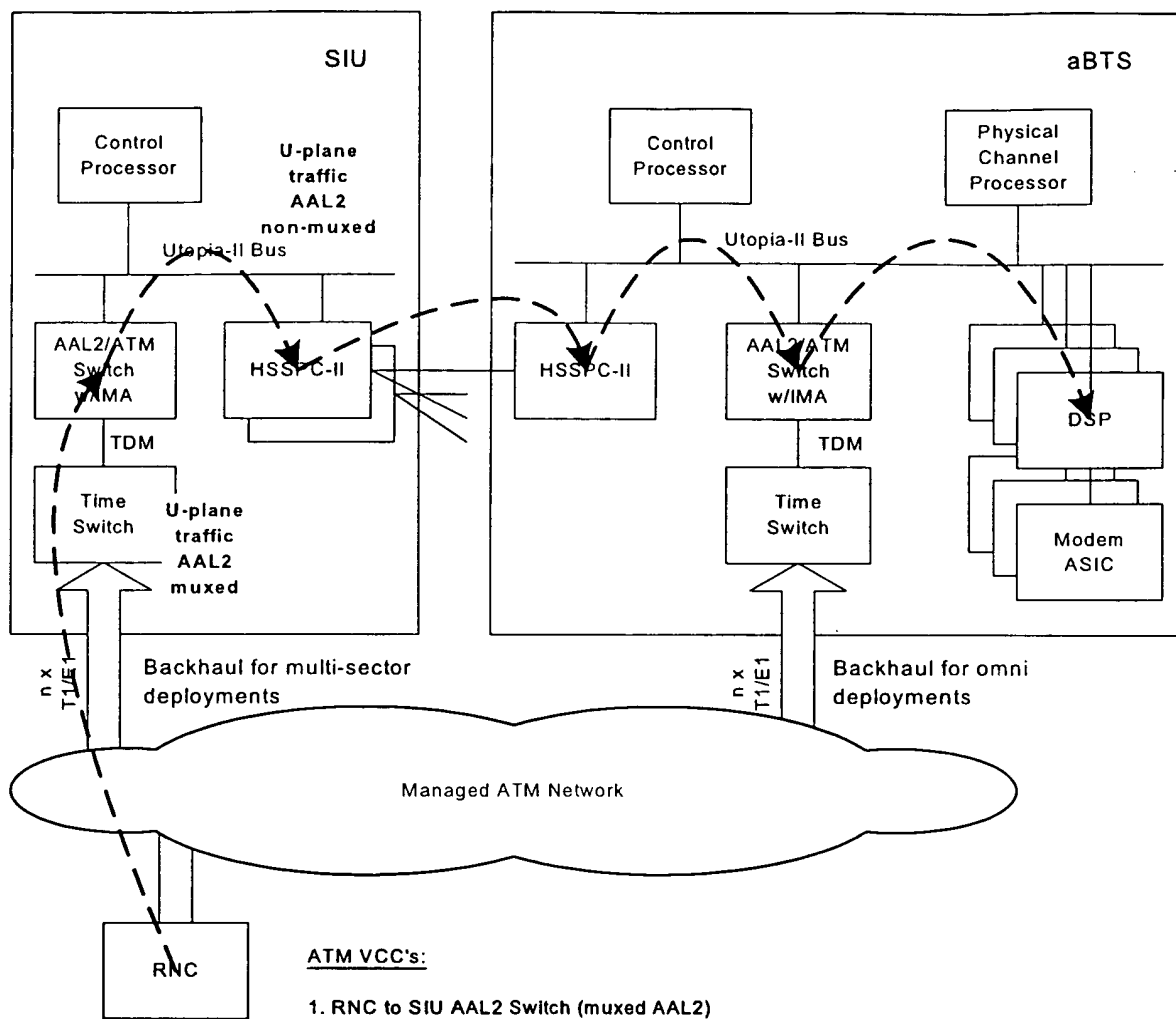


FIG. 35

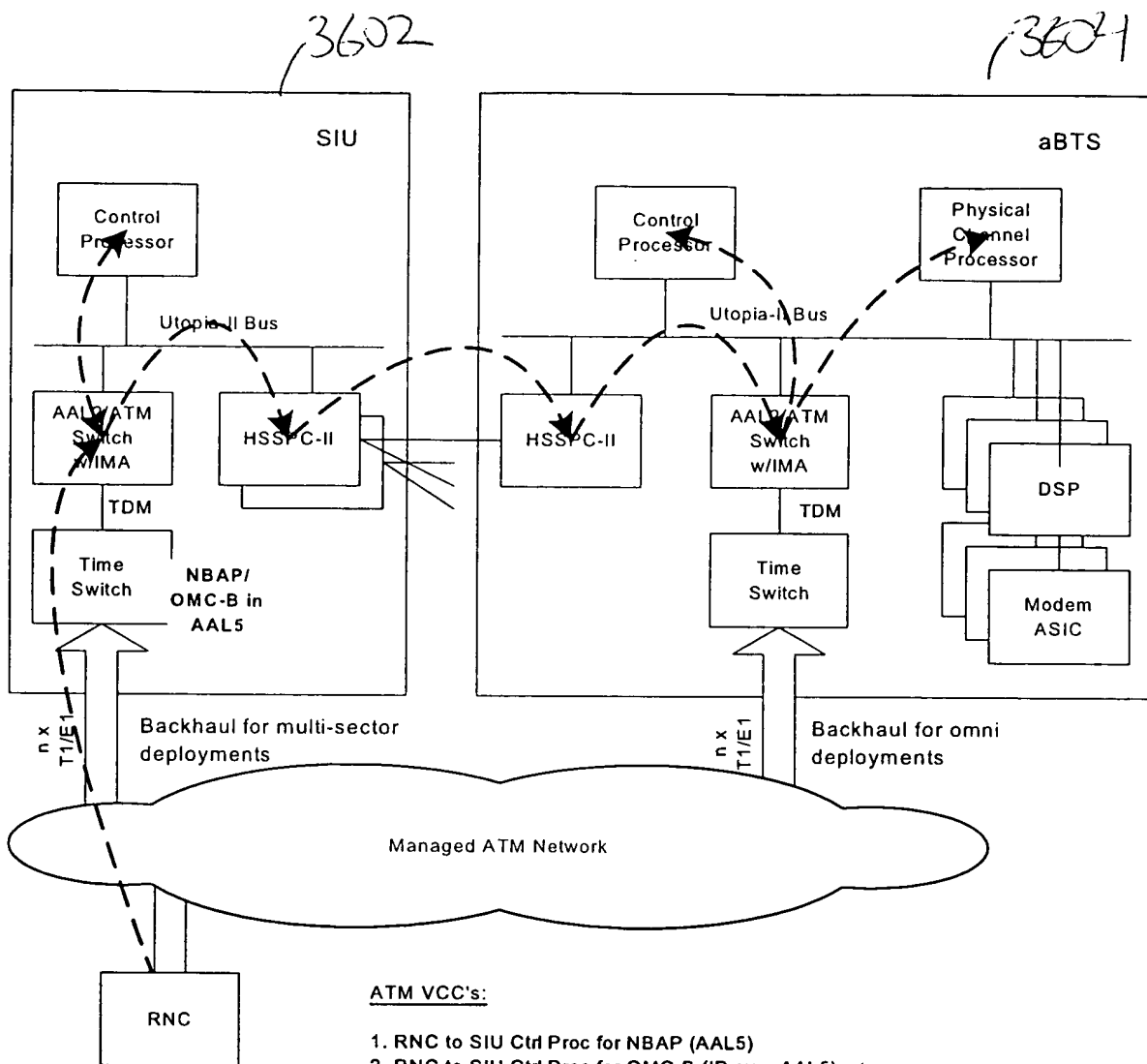


FIG. 36

# UITS '99 (ATM backbone) NBAP Flow

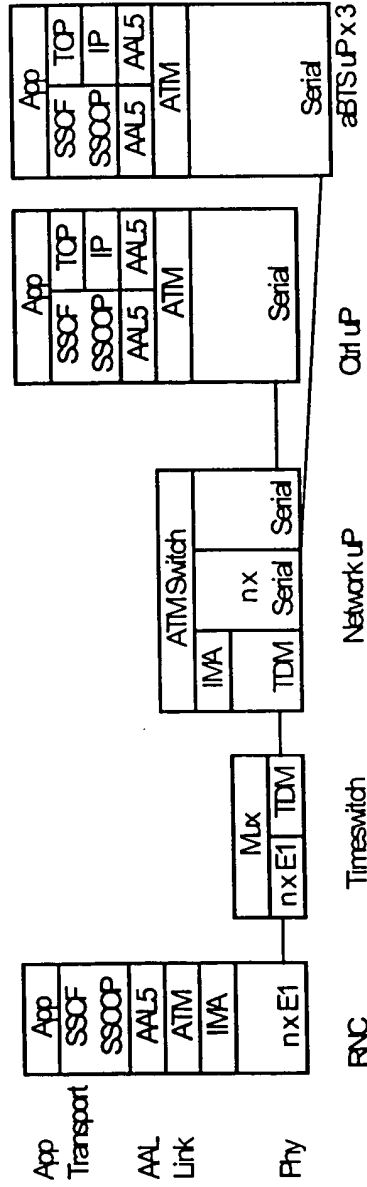


FIG. 37

UMTS '99 (ATM backhaul) OMC-B Flow

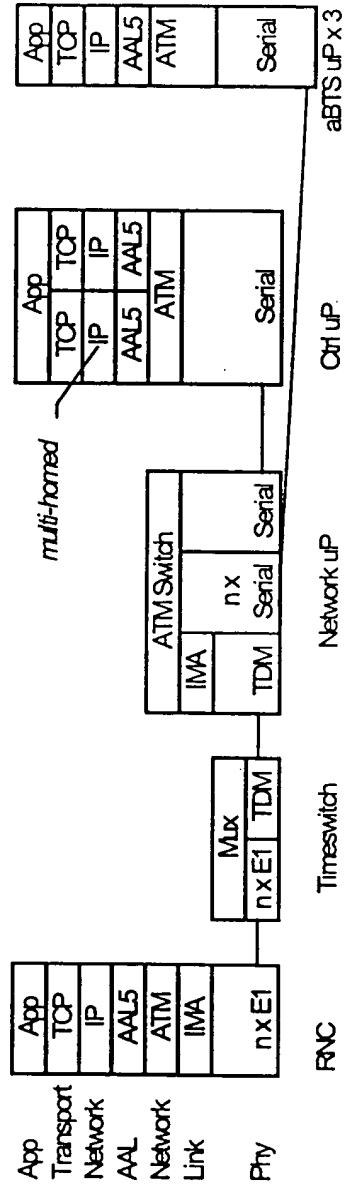


FIG. 38

UMTS '99 (ATM backhaul) User Flow

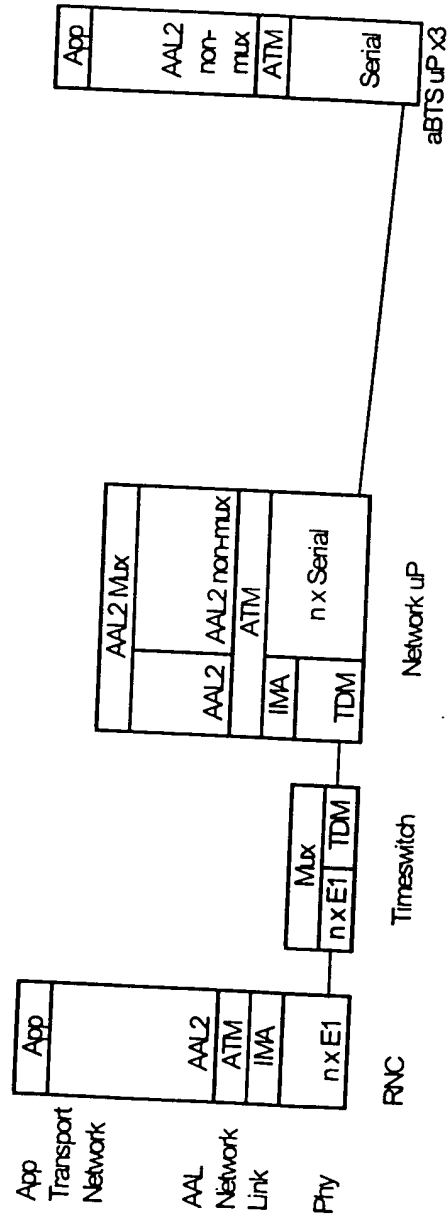
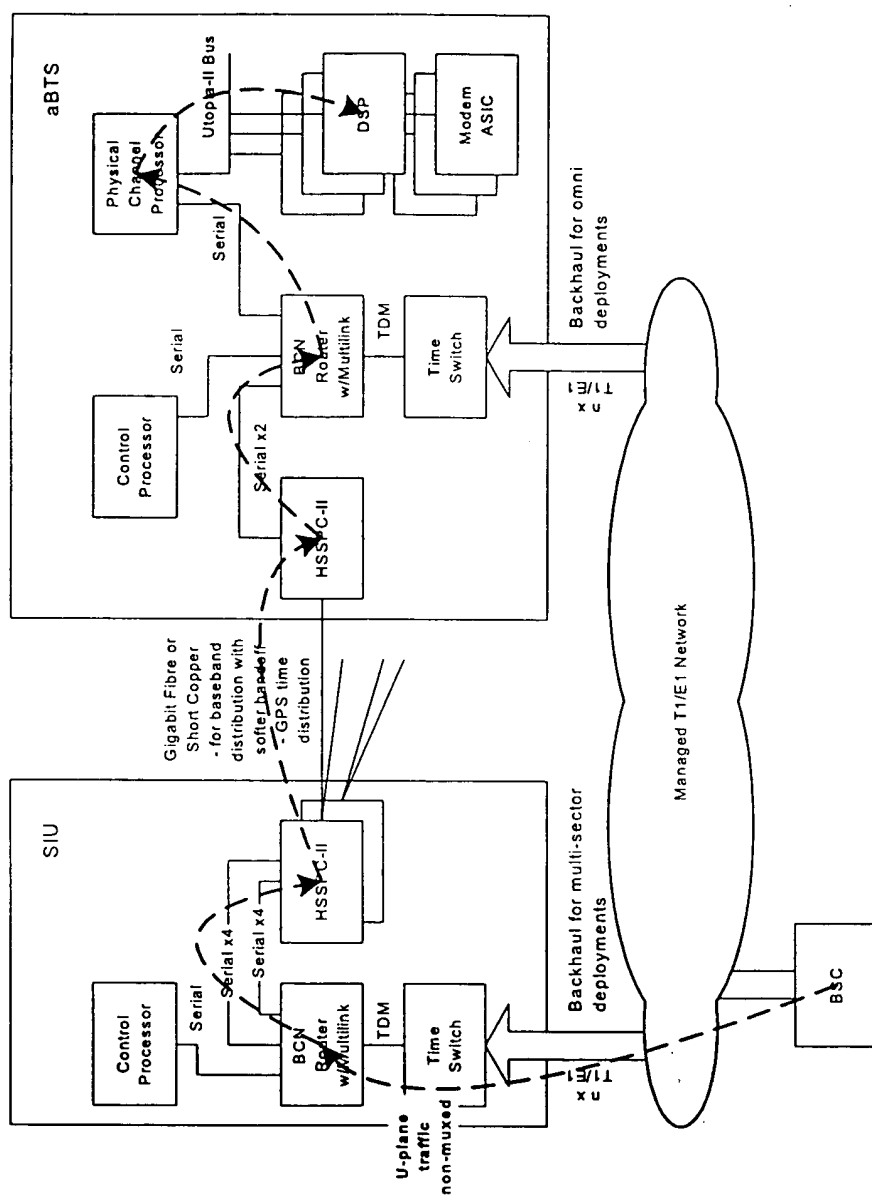


FIG. 39







176

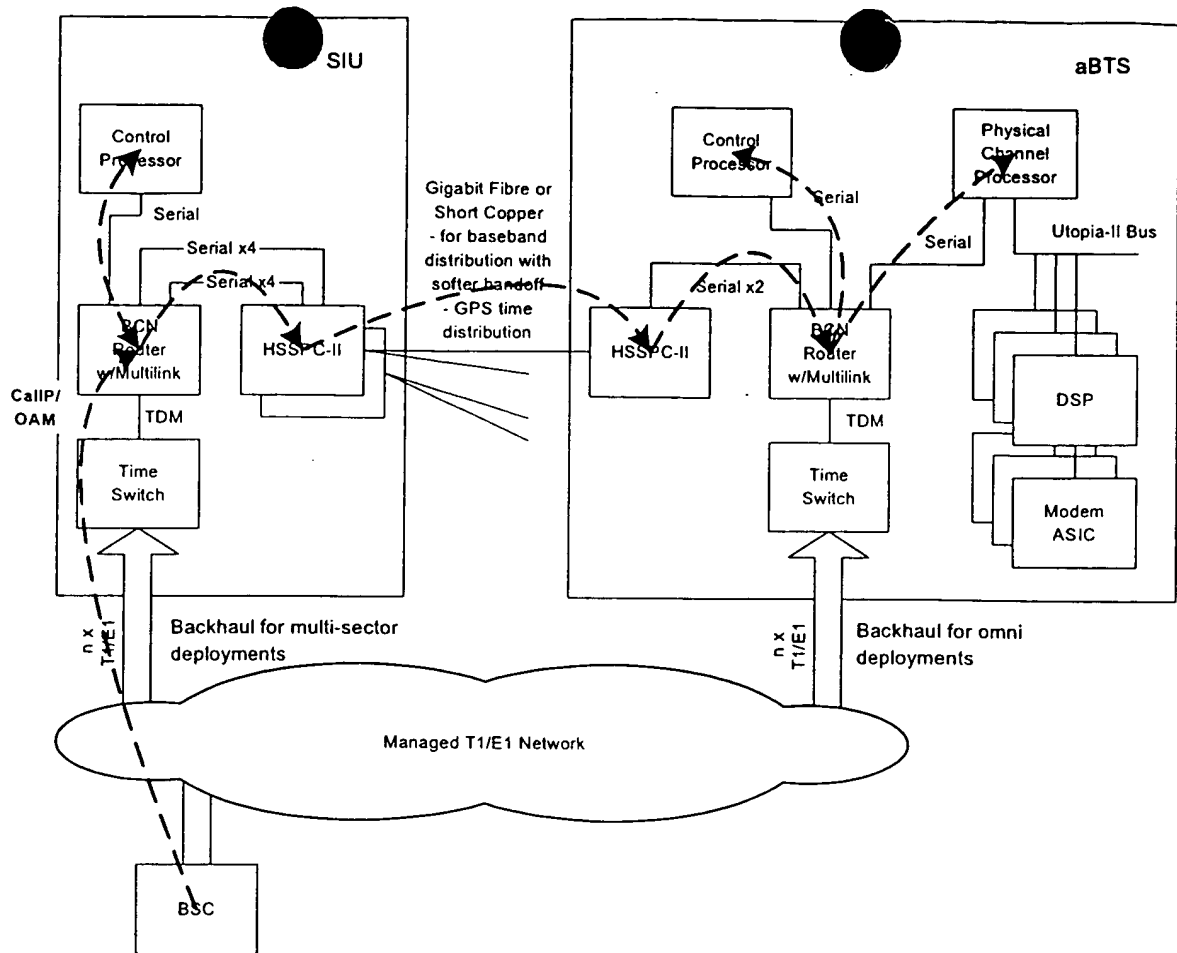


FIG. 42

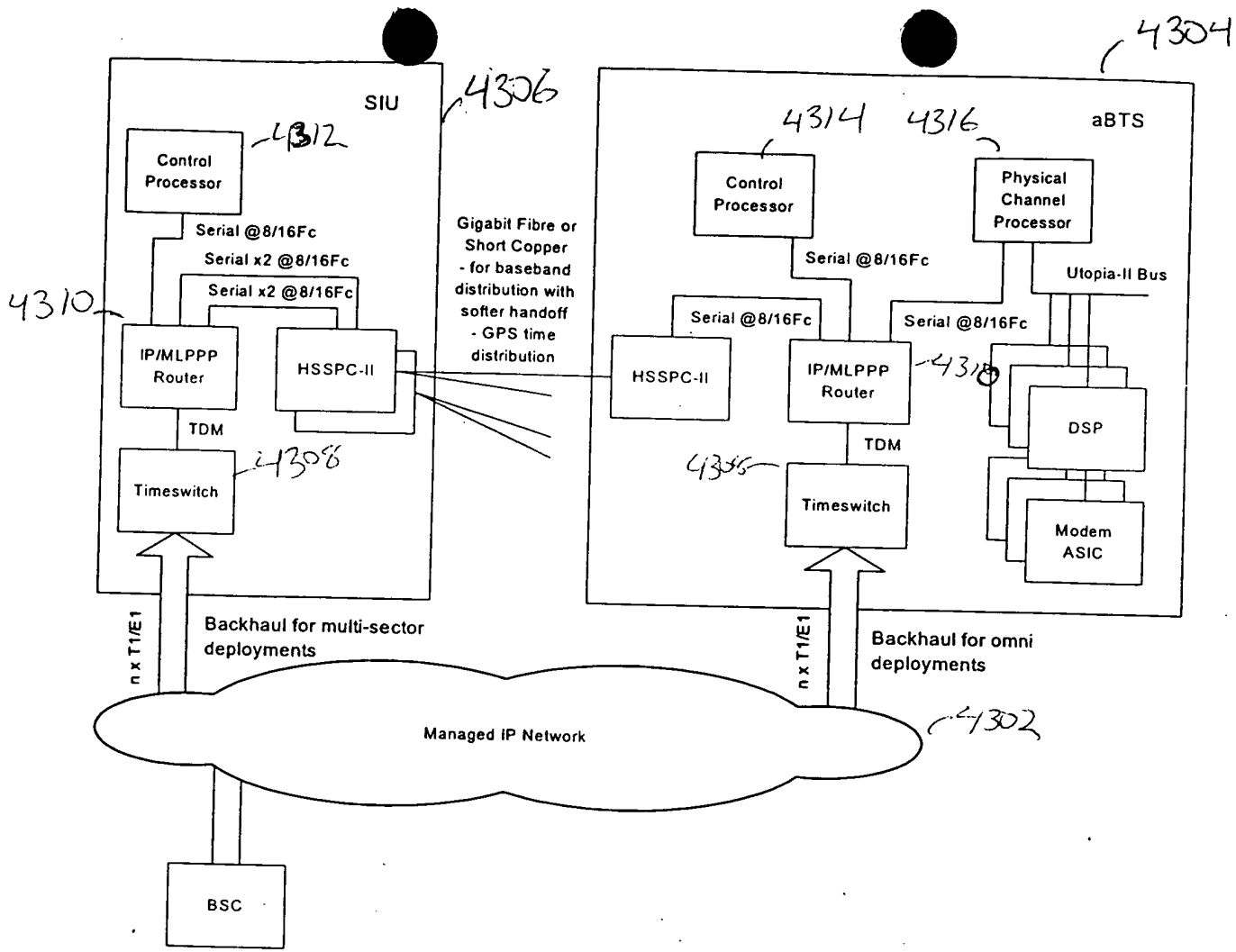


FIG. 43

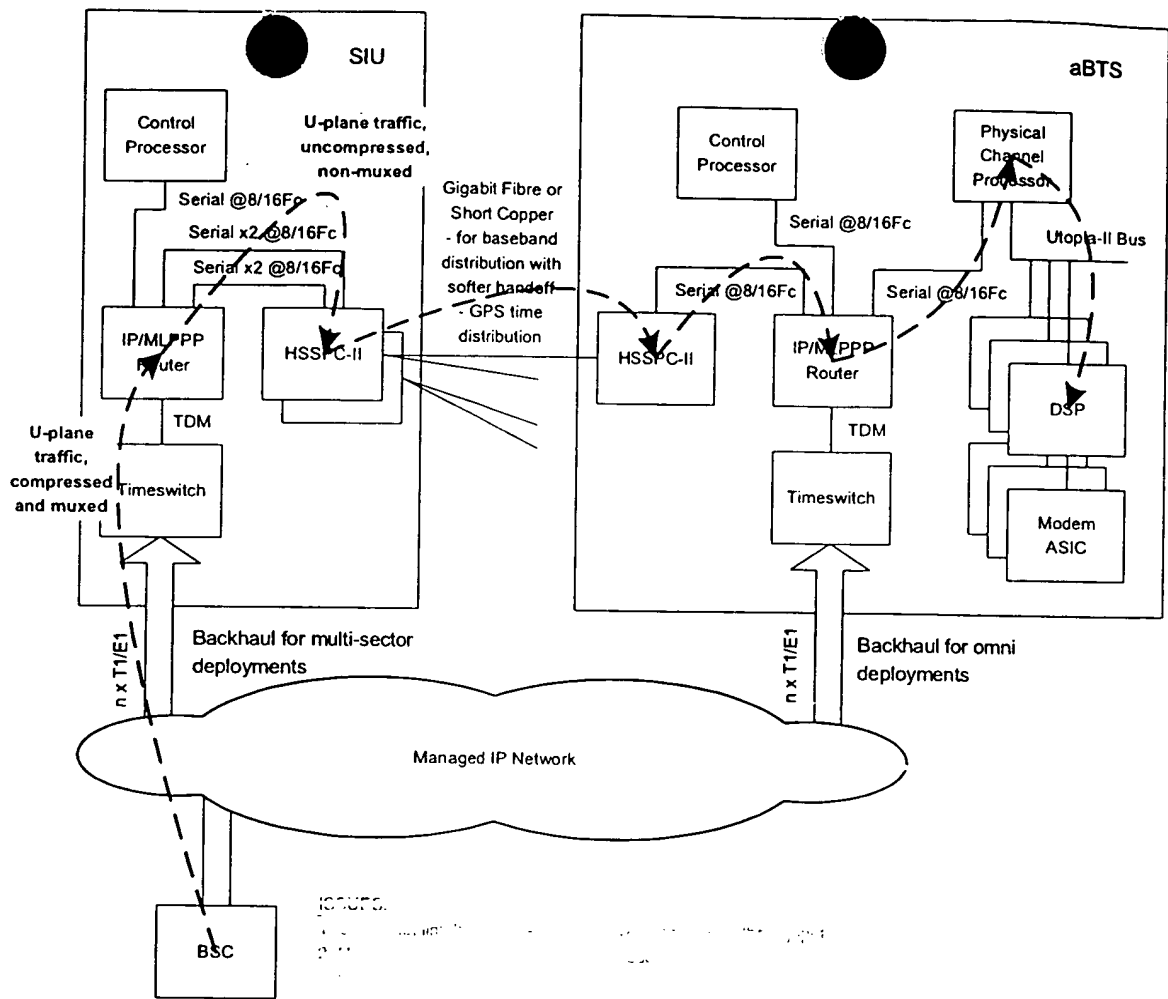


FIG. 44

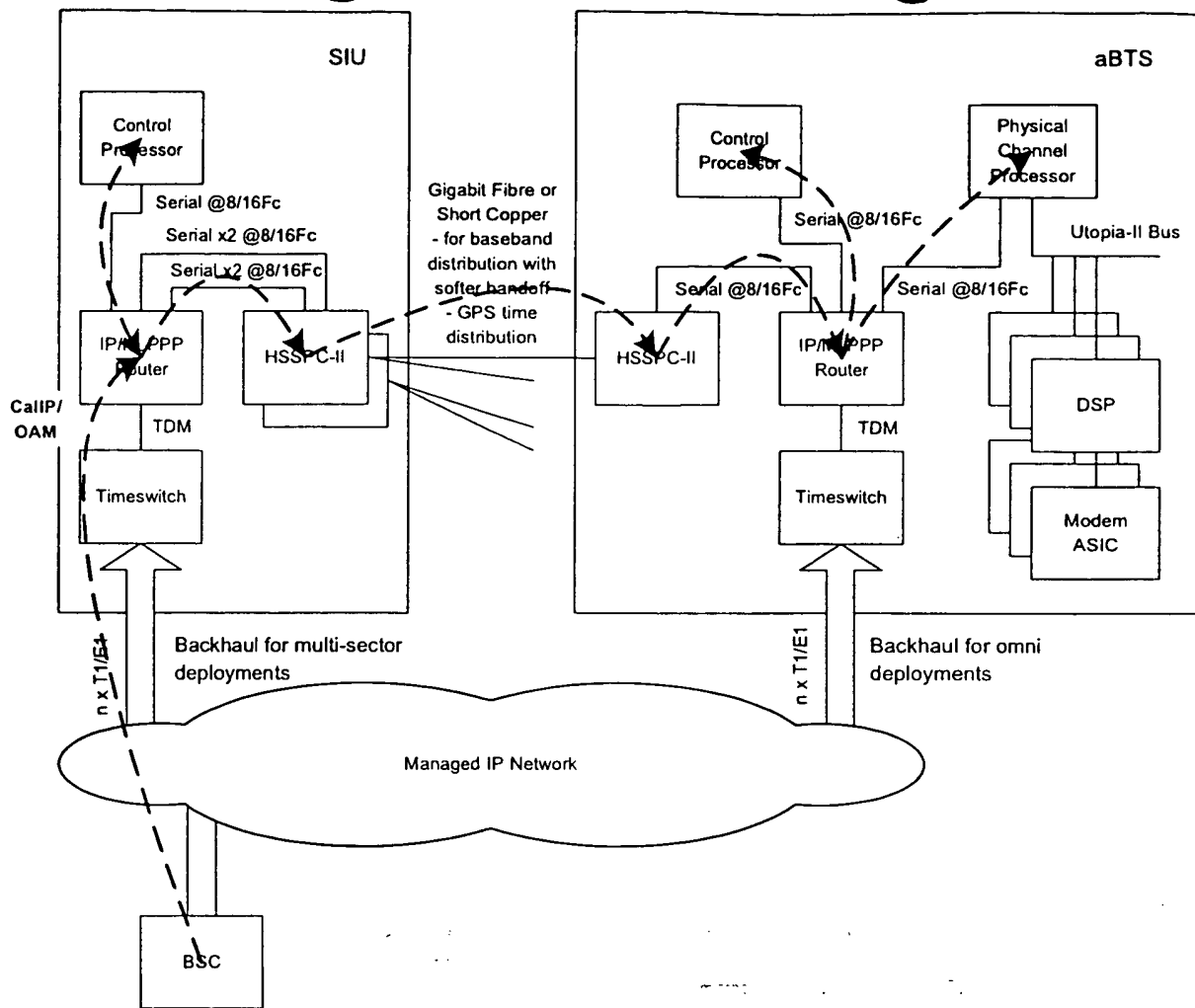


FIG. 45

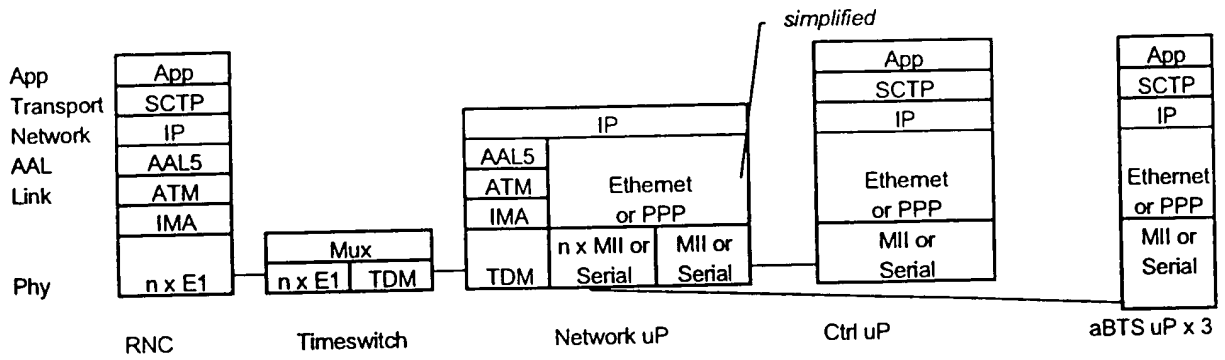


FIG. 46

UMTS '00 (IPoA backhaul) OMC-B Flow / CDMA OAM

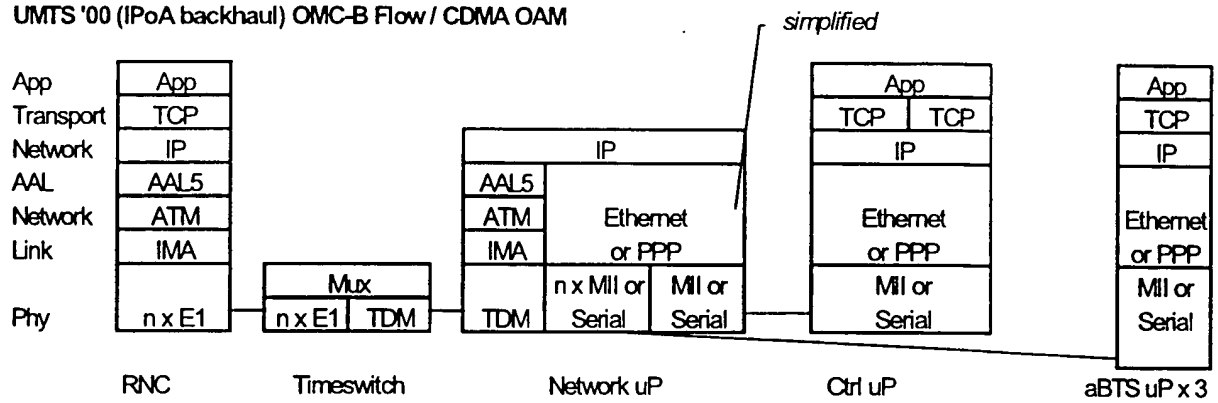


FIG. 47

UMTS '00 (IPoA backhaul) User Flow / CDMA A.bis User Traffic

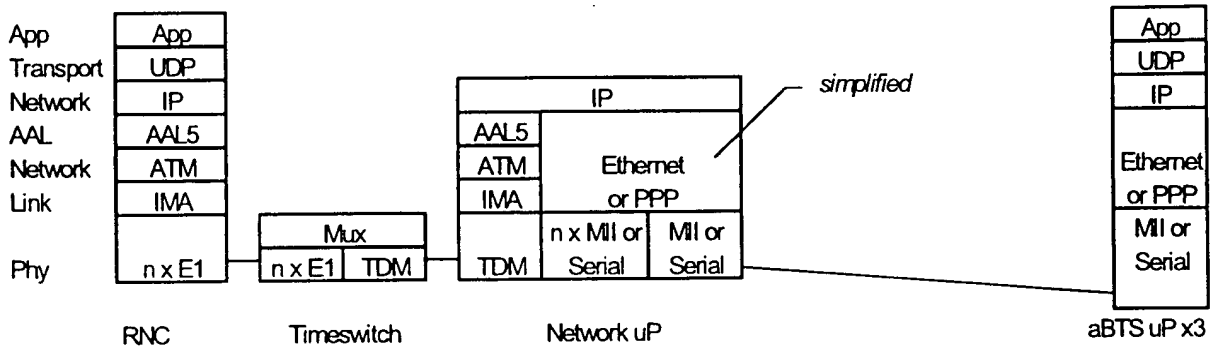


FIG. 48



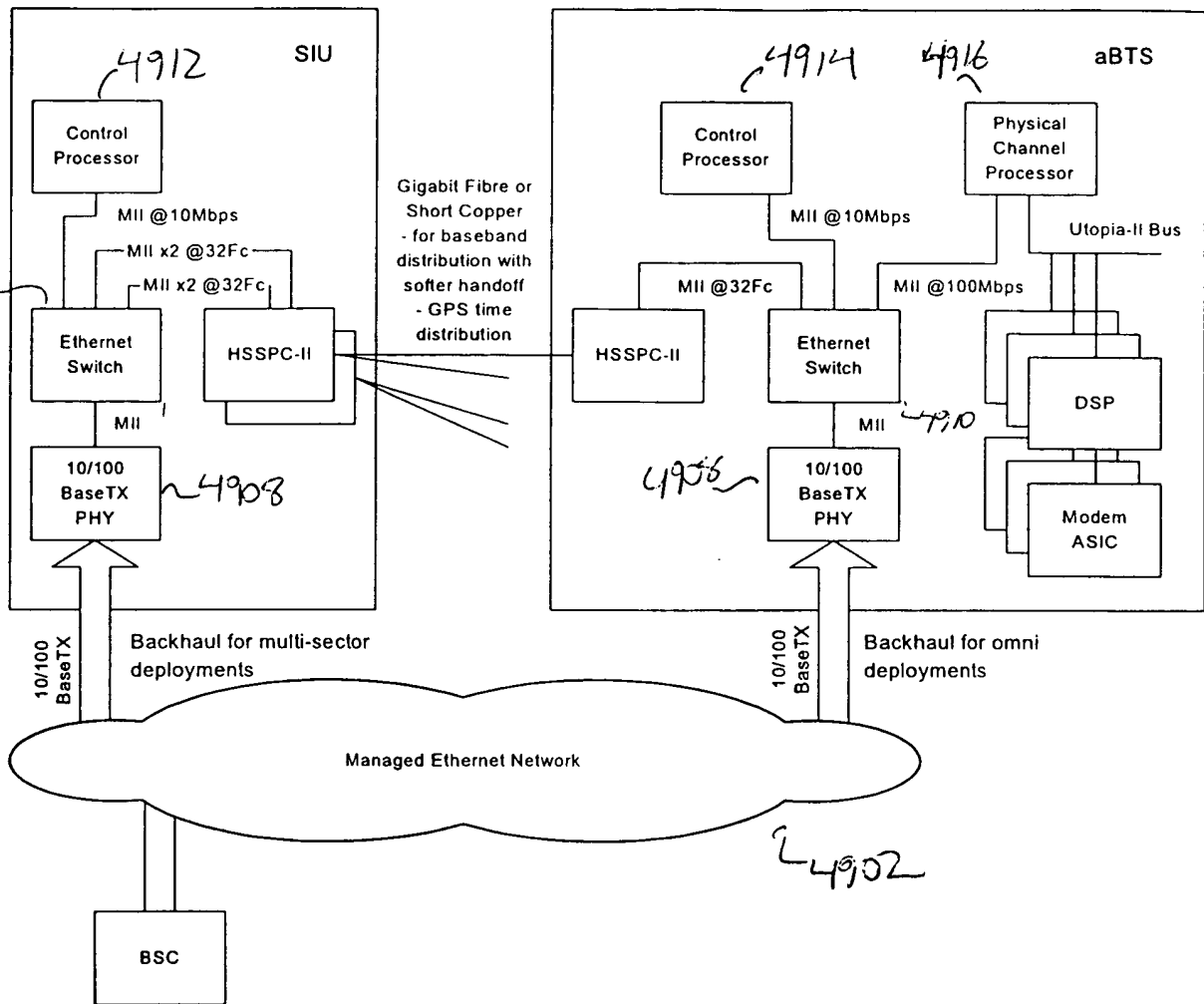


FIG. 49

UMTS '00 (IP/Ethernet backhaul) NBAP Flow / CDMA A.bis

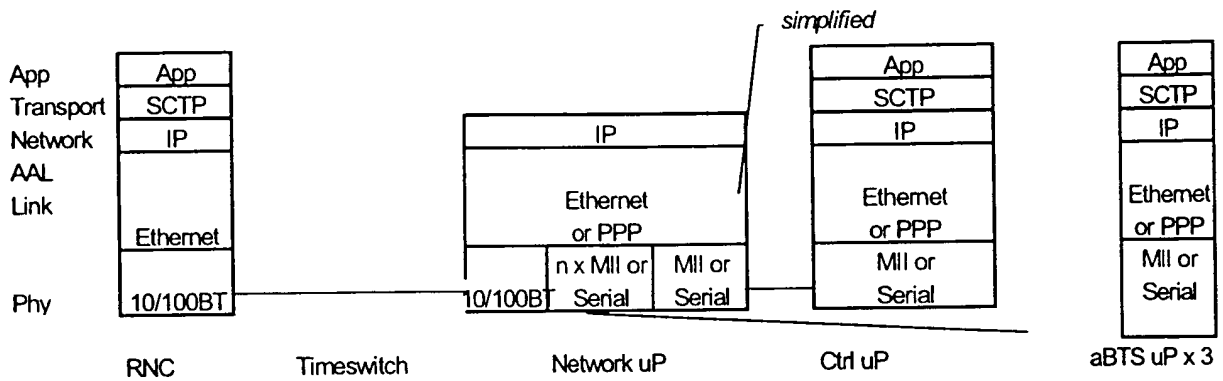


FIG. 50

UMTS '00 (IP/Ethernet backhaul) User Flow / CDMA A.bis

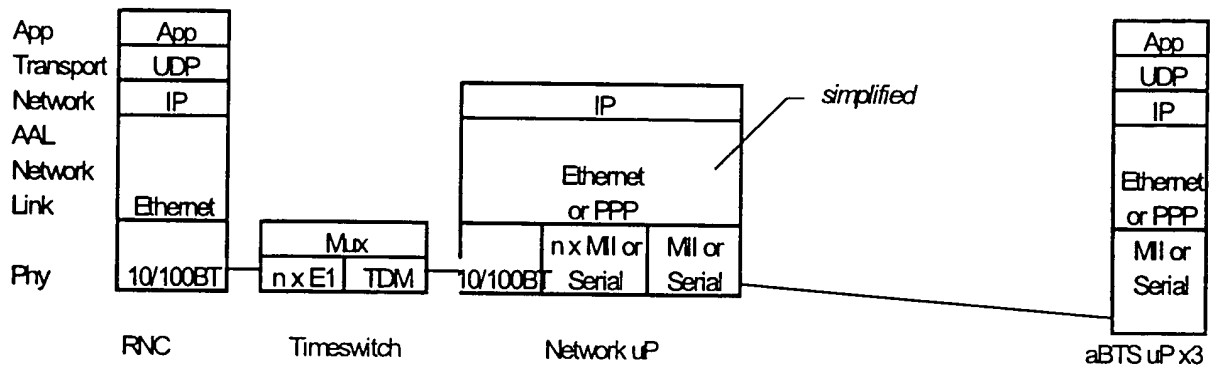
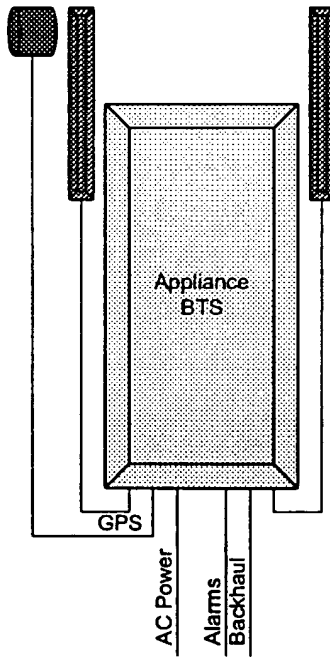


FIG. 51



5202

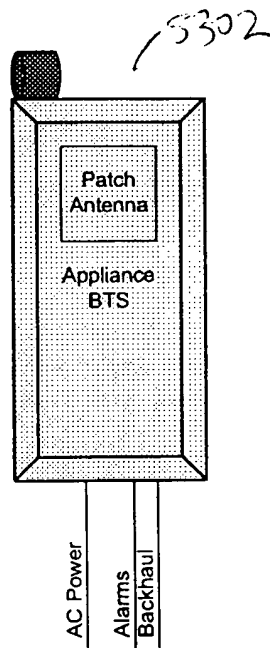


FIG 53

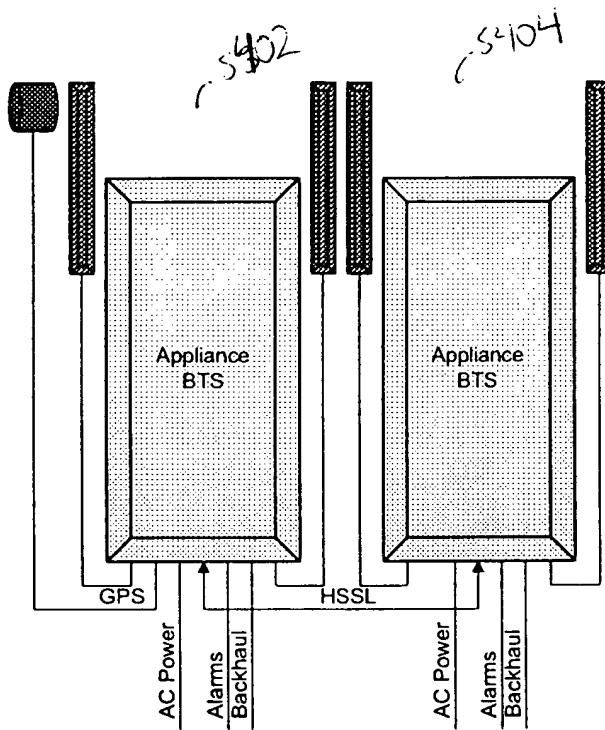


FIG. 54

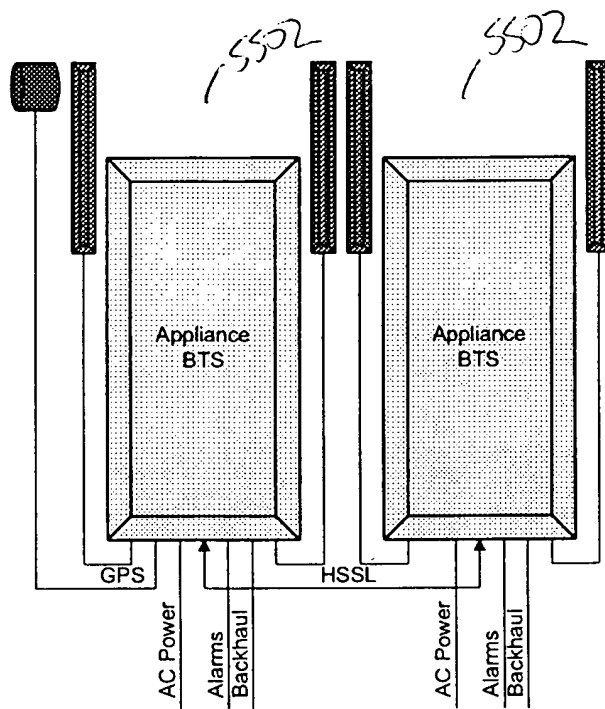


FIG. 55

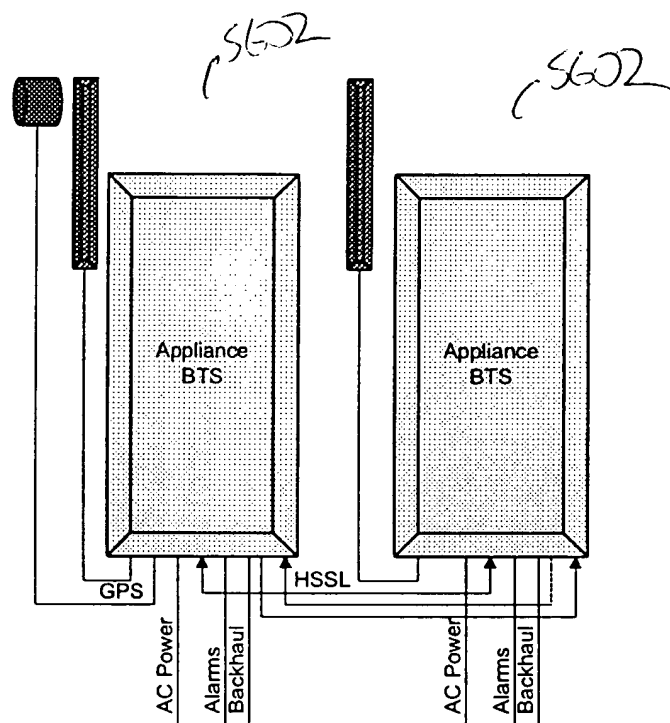


FIG. 56



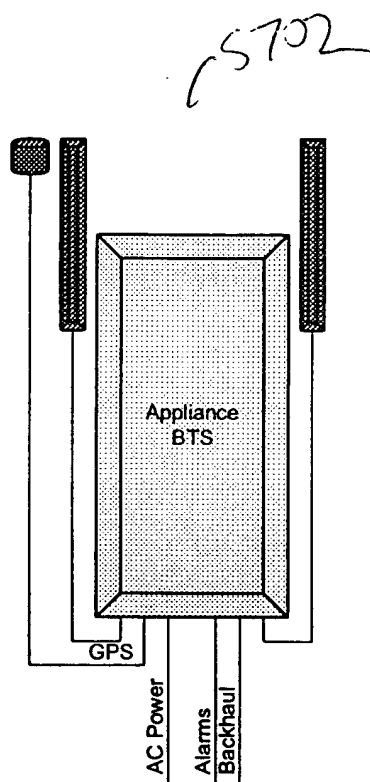


FIG. 57

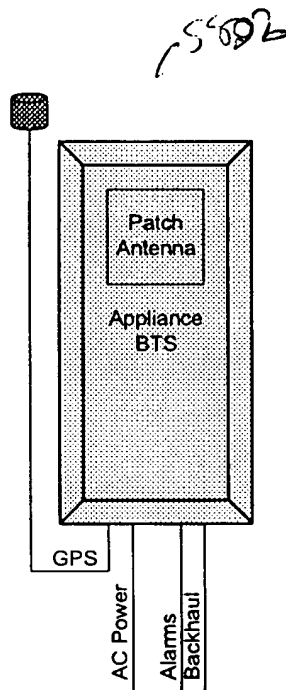


FIG. 58

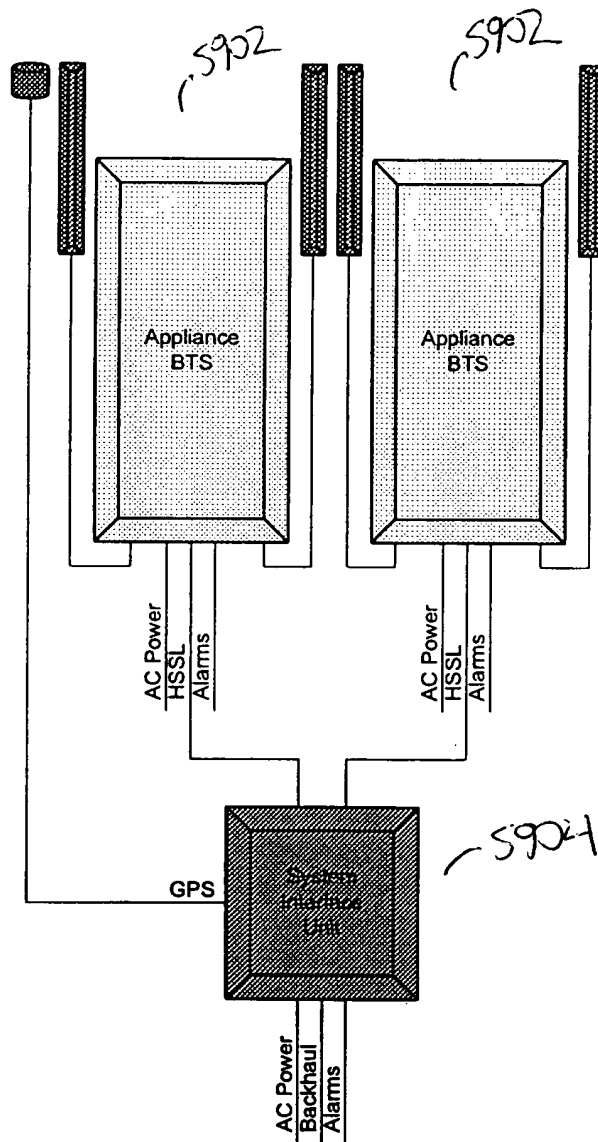


FIG. 59

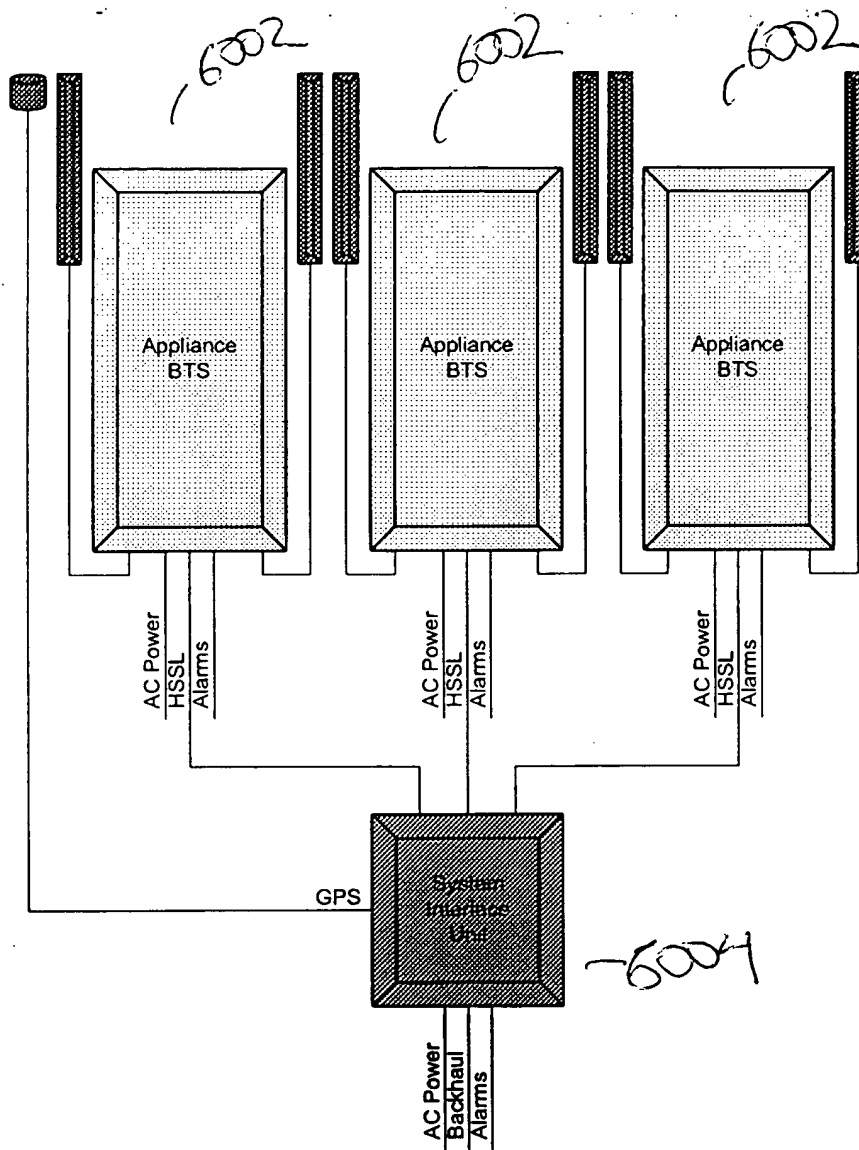


FIG. 60

6102

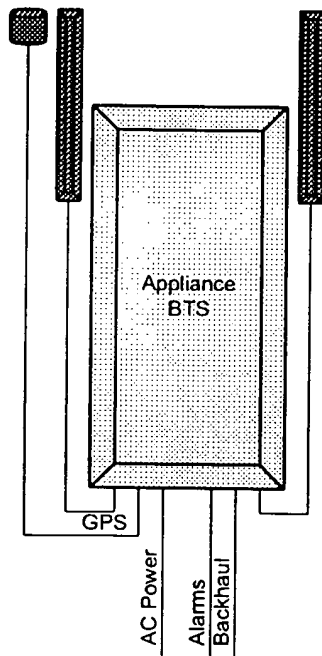


FIG. 61

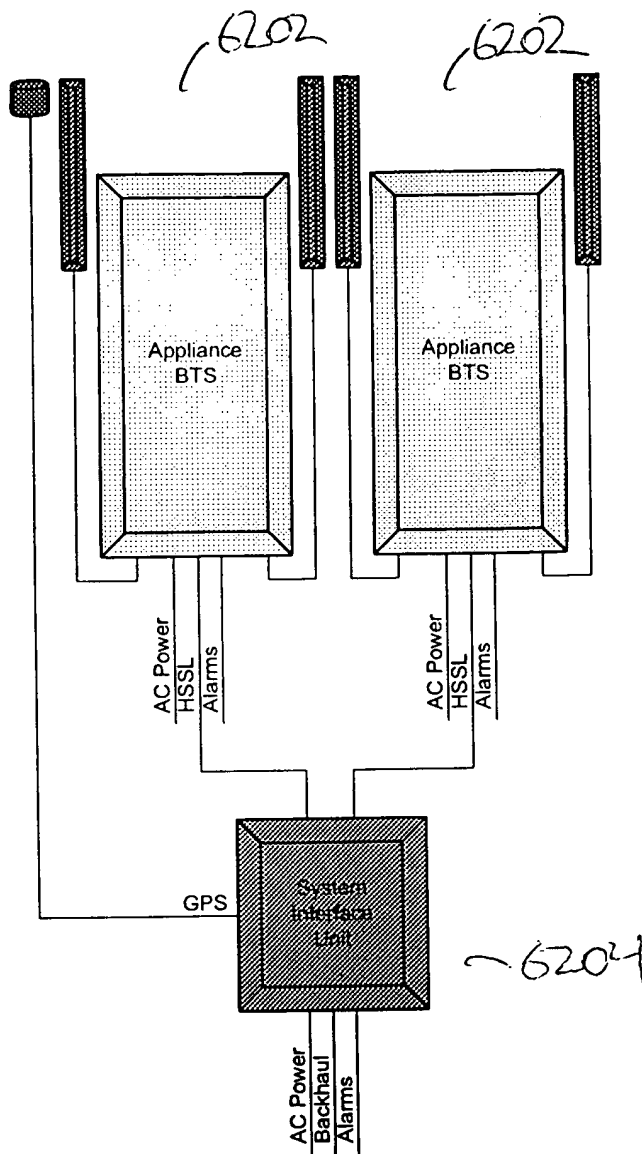


FIG. 62

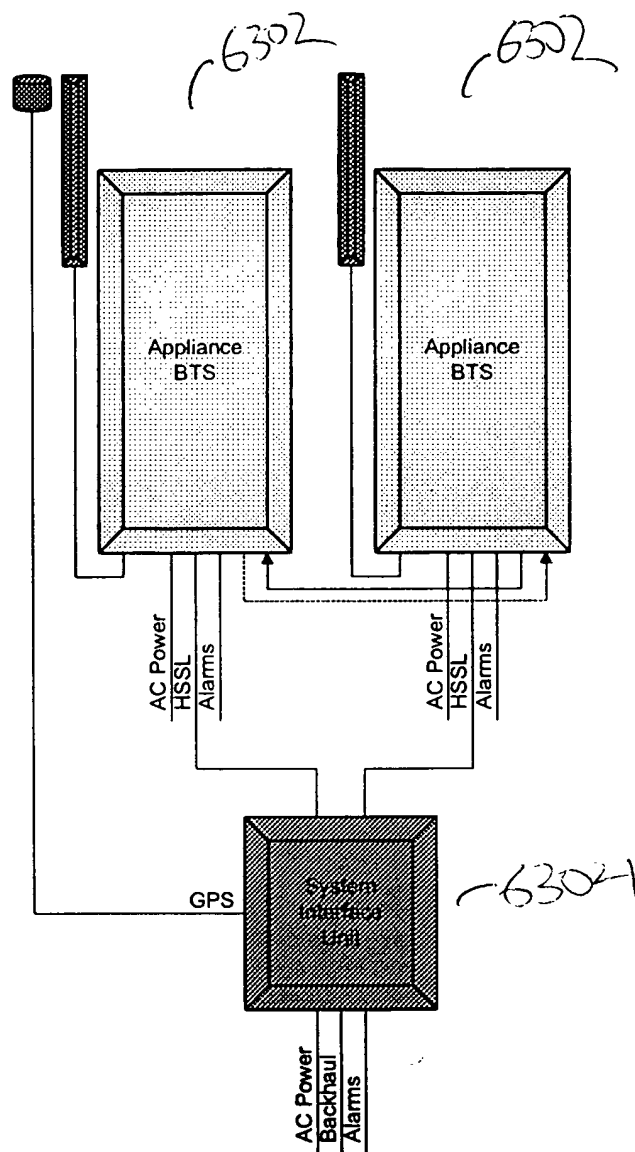


FIG. 63

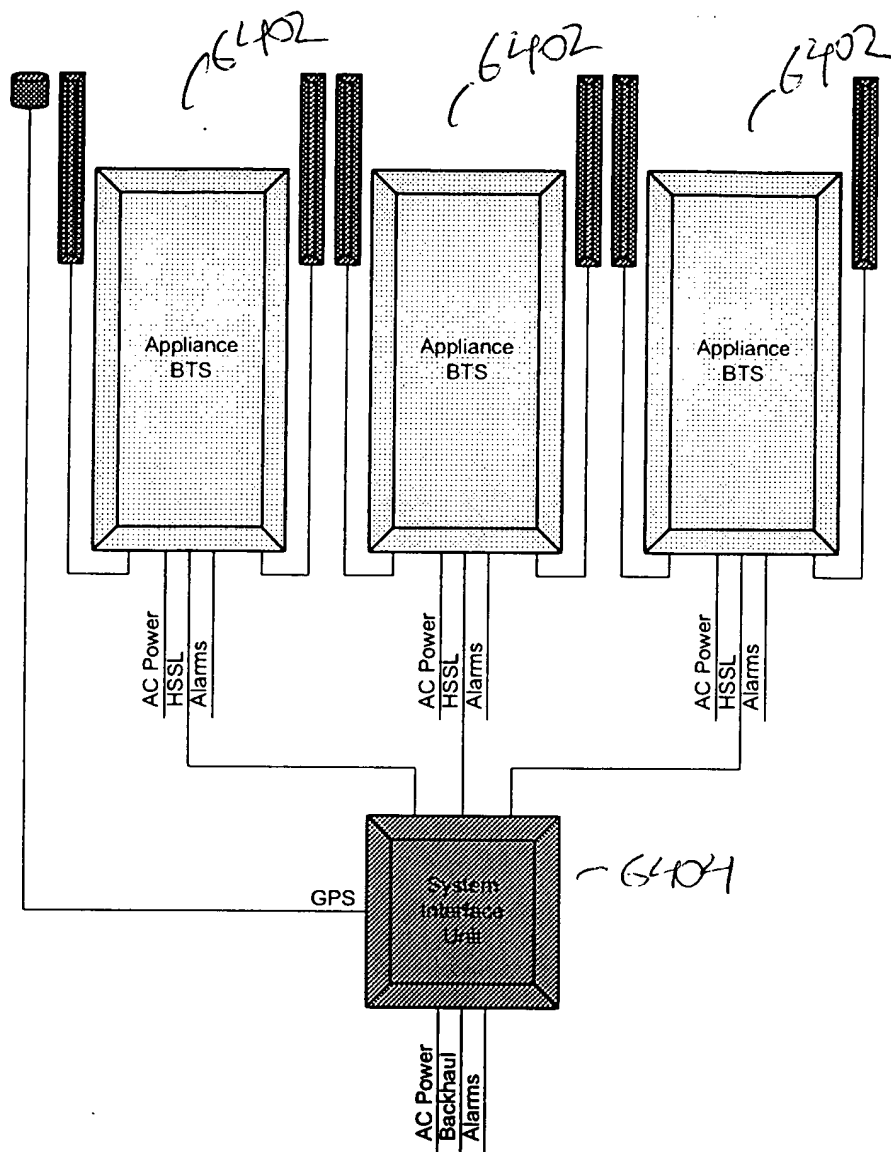


FIG.64



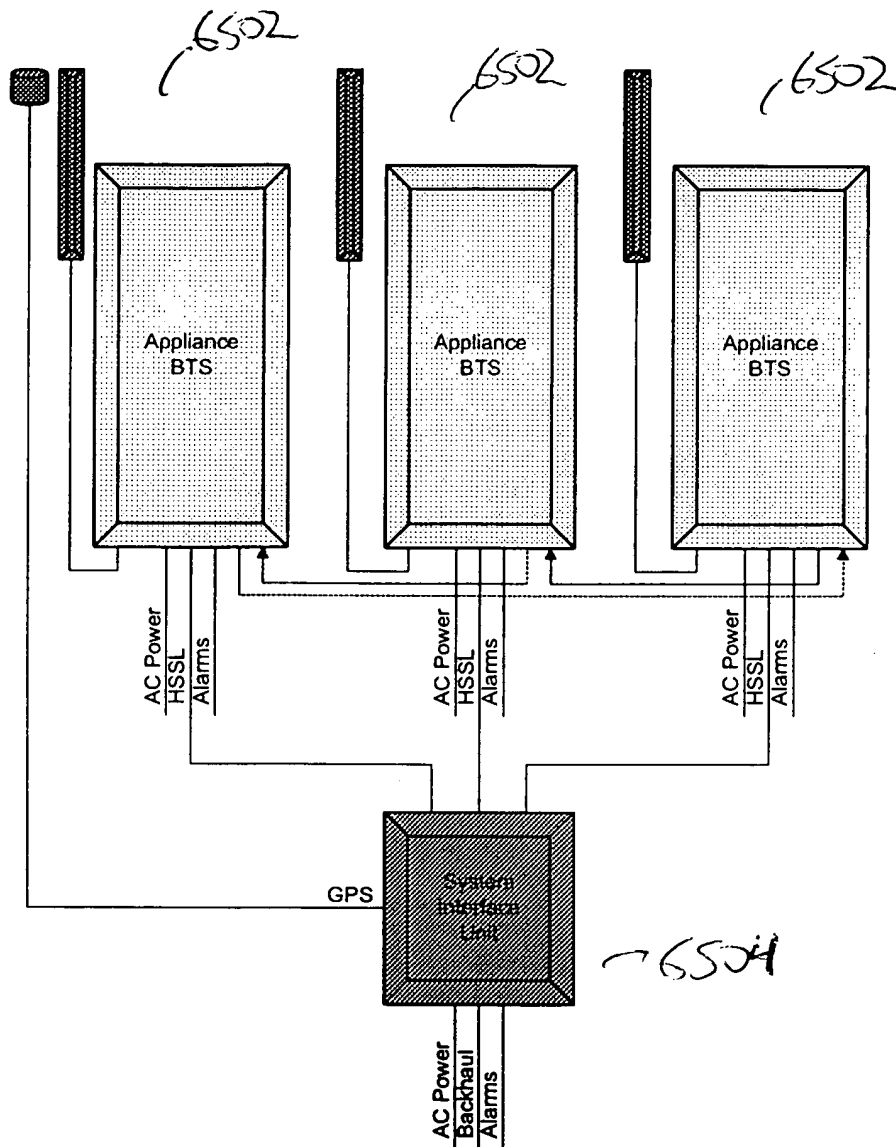


FIG. 65

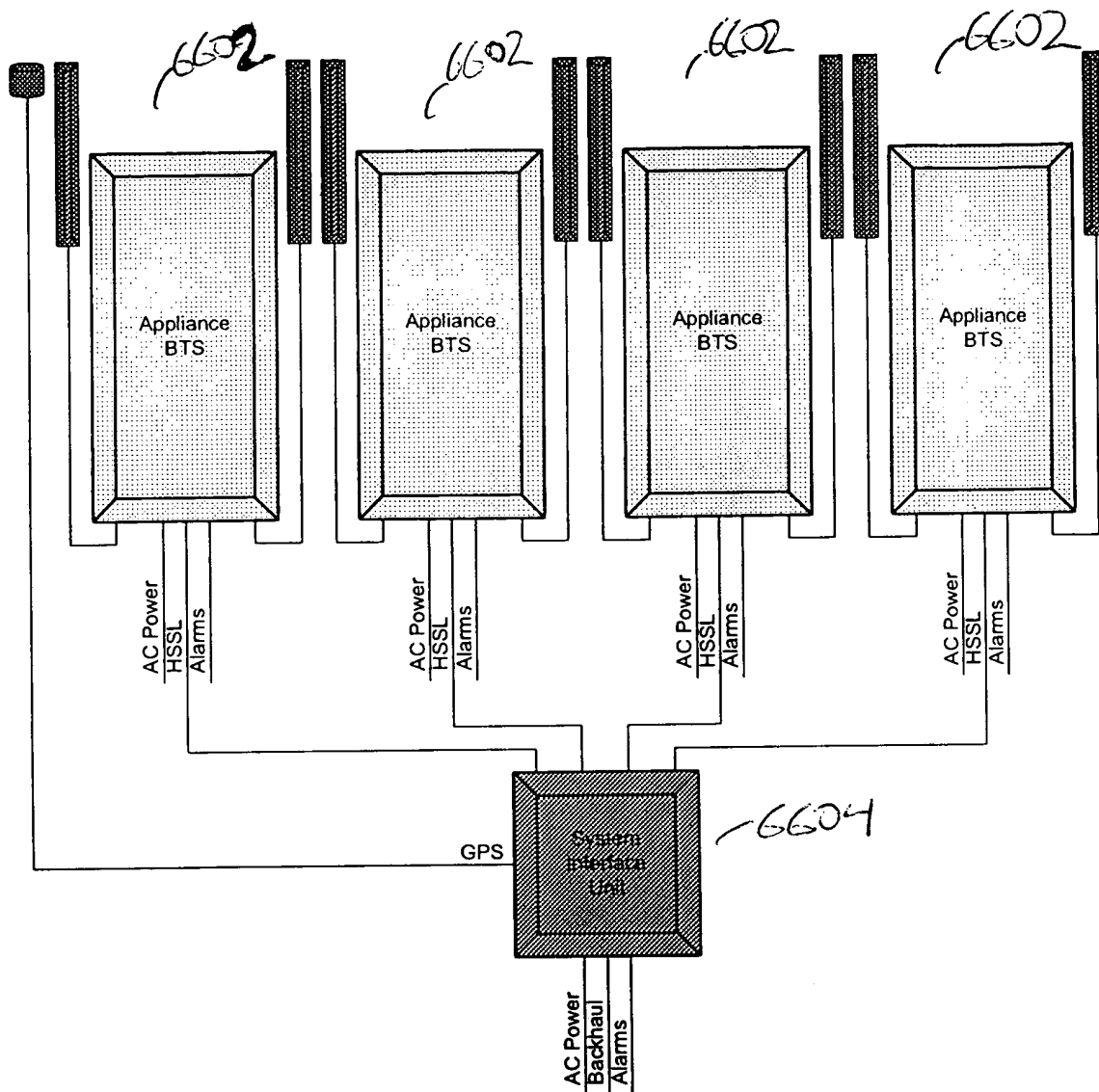


FIG.66

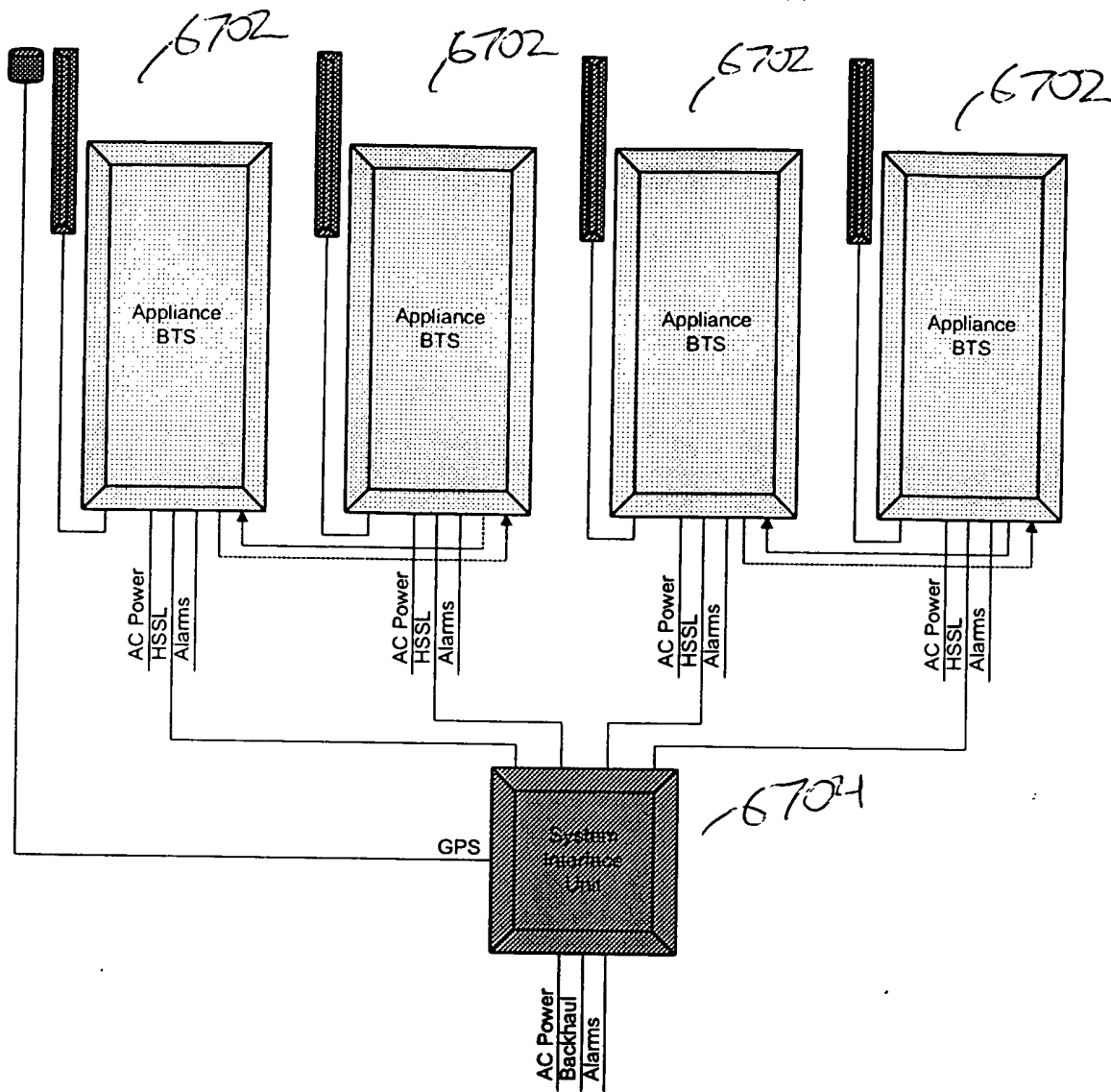


FIG. 67

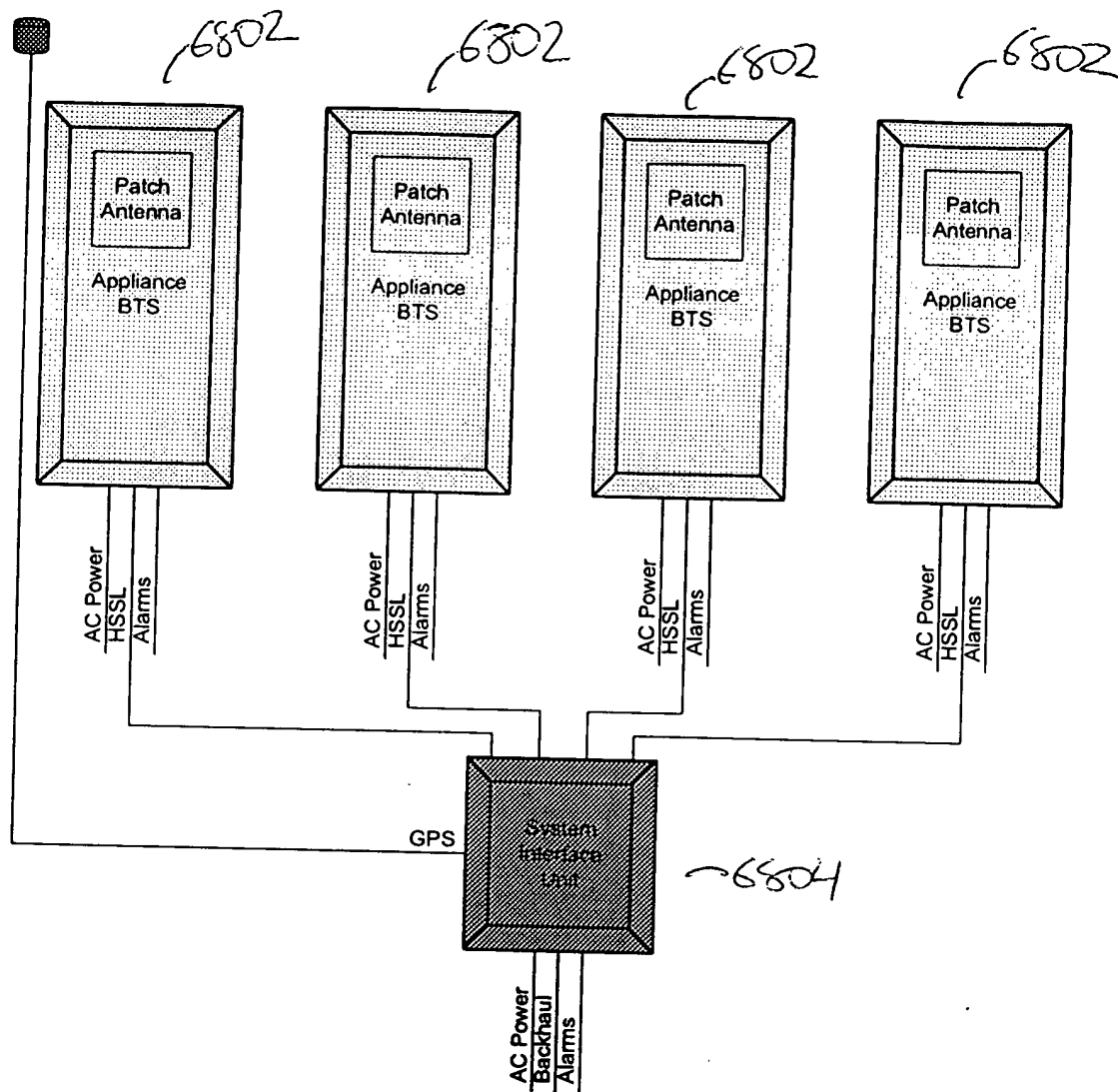


FIG. 68

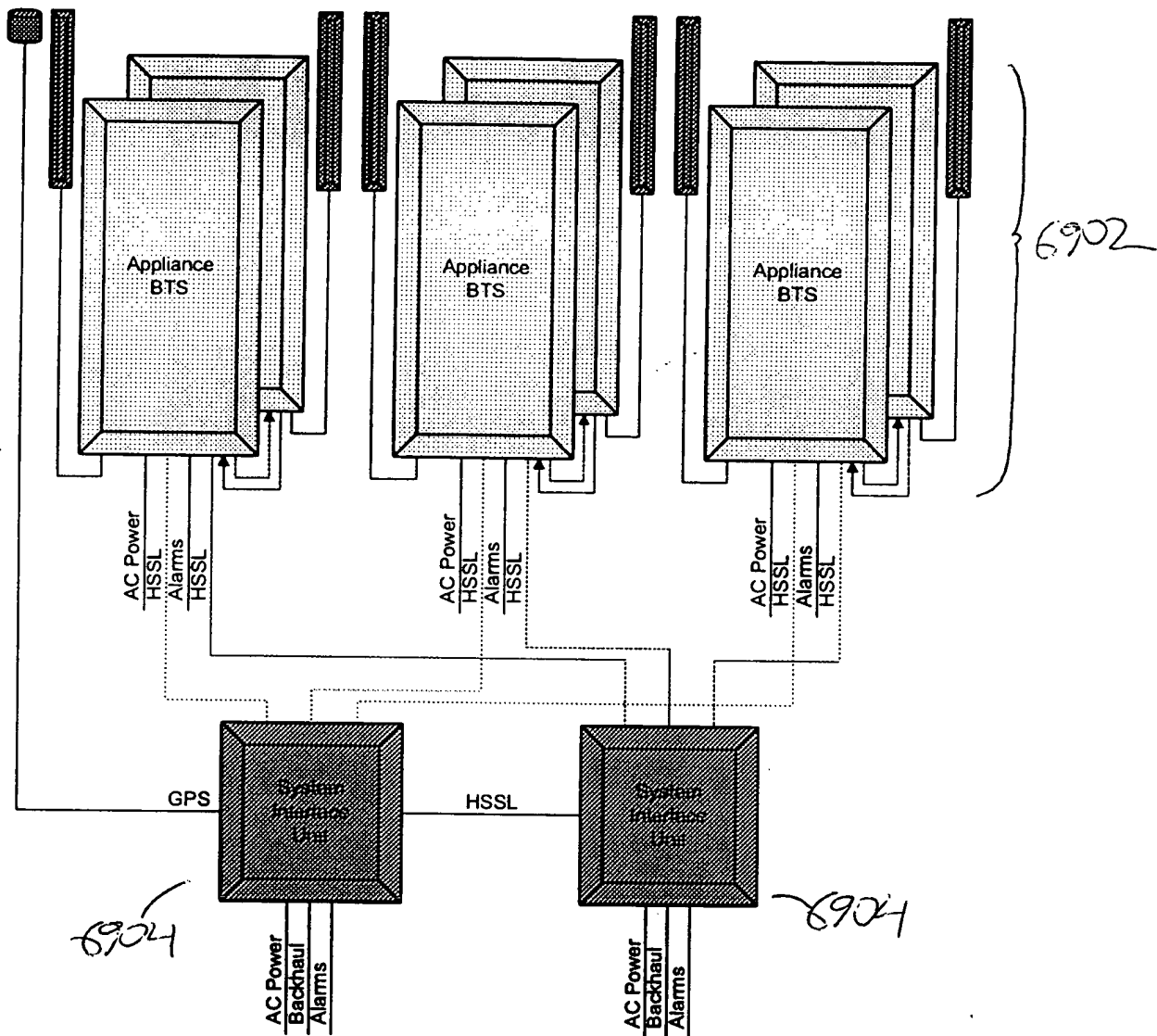


FIG. 69

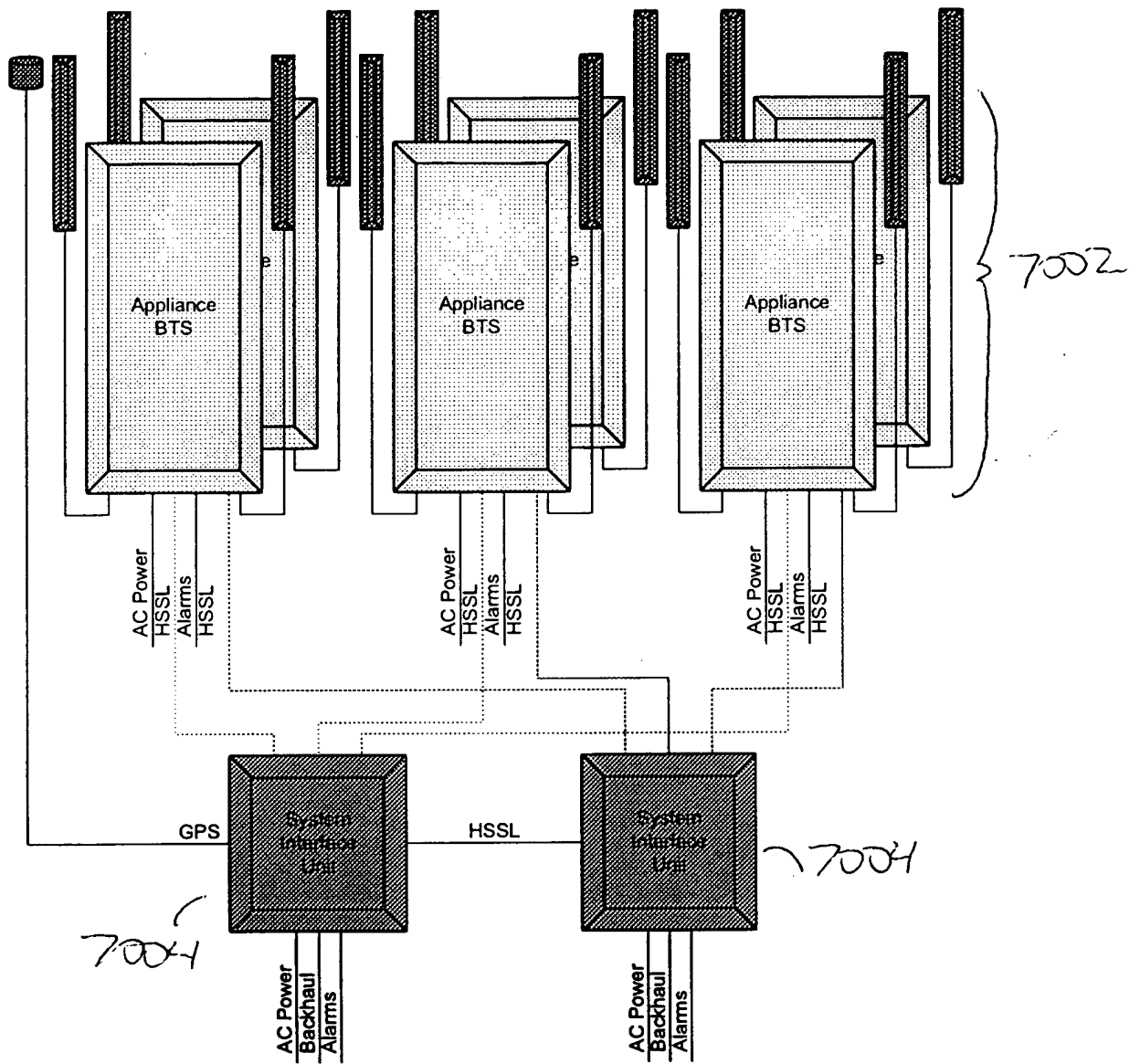


FIG. 70